New Architectures for Low Complexity Scalable Phased Arrays

by

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To my beloved family

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Abstract

Inspired by the unique advantages of phased arrays in communication and radar systems, i.e. their capability to increase the channel capacity, signal-to-noise ratio, directivity, and radar resolution, this dissertation presents novel architectures for low-complexity scalable phased arrays to facilitate their widespread use in commercial applications. In phased arrays, phase shifters are one of the key components responsible for adjusting the signal phase across the array elements. In general, phase shifters and their control circuitry play a significant role in determining the complexity and size of conventional phased arrays. To reduce phased arrays' complexity and size without degrading their performance, two new circuit architectures for scalable phased arrays with a significantly reduced number of phase shifters and control signals are presented. These architectures can be utilized for designing phased arrays in receive as well as transmit mode. The phased arrays designed based on the proposed architectures are intended for applications such as 5G communications and automotive radars for advanced driver assistance systems (ADAS) and autonomous vehicles.

In the first phased array architecture with a reduced number of phase shifters, a vector summation approach is used to integrate the phase shifting function into a new RF feed network to allow the control of signal phase and magnitude distribution along an N-element subarray using a single phase shifter and N variable gain amplifiers. The technique allows for a number of subarrays to be connected to form a larger array to provide a narrow beamwidth. A particle swarm optimization algorithm is also used to maximize the scan range of the N-element subarray

employing a single phase shifter. As a proof of concept, an eight-element transmit phased array operating at Ku band, consisting of two four-element subarrays, is designed and fabricated. The phased array provides 37° of scan range, and is a promising candidate for applications that require a limited scan range such as long-range automotive radars.

In the second phased array architecture also, the phase-shifting function is integrated into the array's feed network through vector summation. A new wide-scan, integrated, scalable phased array with a small size, reduced number of phase shifters, and a simplified control mechanism is designed and fabricated at K-band in 130-nm CMOS process. In the designed wide-scan (±90°) phased array, the total number of phase shifters and analog control signals are reduced by a factor of two compared to the conventional phased arrays. This phased array is a promising candidate for short-range automotive radars that require a wide scan range. The control complexity, chip size, and power consumption of this phased array can be further reduced if it is intended to operate as a limited-scan phased array.

Furthermore, two new circuit topologies for integrated low-power vector modulator phase shifters with small size and simple control are also presented. The first phase shifter is based on a new analog vector modulator circuit where the phases of the orthogonal vectors I and Q are varied in conjunction with their amplitude ratio, all by adjusting a single variable, hence enabling control of the vector sum phase while limiting its magnitude variation. All the tasks of vector generation, vectors' amplitude and phase variation, and vector summation are performed in a single stage to save power and area. The second phase shifter is a frequency-tunable 360° analog CMOS vector modulator circuit with an adjustable output amplitude operating at K and Ka bands. Due to its adjustable output amplitude, the phase shifter can allow accurate control of beamwidth and sidelobe levels. In the circuit topology of this phase shifter, all the tasks of a vector modulator

(vector generation, gain control, and vector summation) are performed in a single stage occupying a very small area among the phase shifters with comparable performance. The phase shifters designed within this work provide a continuous phase tuning, are compact in size, and have simple control circuitry.

Chapter 1: Introduction

A phased array is an ensemble of antennas capable of beam forming and steering by adjusting the relative phase and amplitude of the signals received or transmitted by each antenna element. Due to the spatial selectivity offered by phased arrays, they reduce co-channel interference, multipath fading, and the required transmit power in telecommunication systems. Phased arrays also increase channel capacity and data rate without requiring extra bandwidth and enhance cross-range resolution and signal-to-noise ratio in radar systems [1]. These unique features have made phased arrays very attractive for a broad range of applications in communication and radar systems since the advent of this technology.

Phased array antennas have traditionally been used in aeronautics, defense, and satellite communication systems for several decades. Recent ongoing advancements in communication systems and radar-based sensors have built up an increasing interest in utilizing phased arrays for low-cost commercial communication and radar systems in diverse areas such as advanced driver assistant systems (ADAS) and 5G communications.

Despite the wide range of phased array applications, their complexity, size, and cost have remained as challenges for the widespread use of phased arrays in low-cost commercial applications. Therefore, many works have focused on reducing phased arrays' complexity and size. This chapter presents the history, operation principles, and advantages of phased array in transmitters and receivers, along with their current and emerging applications. The conventional designs of phased arrays and the main sources of their complexity and size are also presented in this chapter. Moreover, various approaches proposed to reduce phased arrays' complexity are

discussed. Finally, an overview of thesis presenting two new architectures and design techniques for low-complexity scalable phased arrays along with two new circuit topologies for low-power vector modulator phase shifters with small size and simple control is provided at the end of the chapter.

1.1 History of Phased Array Antennas

Increasing antenna directivity for long-range communications has been the subject of a plethora of research since 1906 when Marconi published a paper on directive antennas [2]. The first demonstration of an enhanced radio wave transmission in one direction which can be viewed as the outset of phased array technology was provided by Nobel laureate Karl Ferdinand [3]. Several solutions for high gain directive antennas with fixed beams have been developed by mid 1930s. Afterward, many researchers focused on design of antennas with steerable narrow beams (which allow for receiving signals as their direction of arrival changes) for radar applications. The first steerable antenna was developed by Friis and Feldman in 1937 for shortwave reception. In this steerable antenna array, shown in Fig. 1.1, mechanical phase shifters were employed to

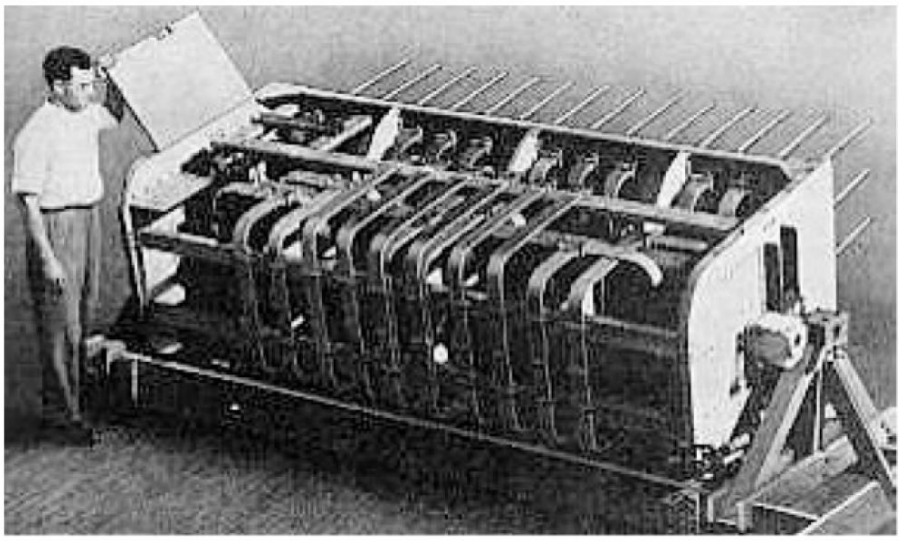


Fig. 1.1. Steerable antenna array for shortwave reception developed by Friis and Feldman

provide the required phase progression across the array elements. To address the military demands during World War II, Nobel laureate Luis Alvarez presented the first electronically steered array at MIT Radiation Lab [4]. He used phased arrays in a fast beam steering radar system for facilitating the landing of aircrafts. At this time, due to the advantages of beamforming and beam steering of phased arrays including rapid beam scanning and robustness toward jammers and clutter, they were developed mainly for radar applications. After the war, phased array technology was developed on both sides of the Iron Curtain with a focus on the electronic phase shifters as the key element of electronically steerable arrays. This led to improving arrays' performance and size [5] – [11]. Phased arrays' applications were later extended beyond military radars [12] – [14], and arrays were adopted for other applications such as radio astronomy (by Nobel Prize winners Antony Hewish and Martin Ryle [15]) where the signals from several antennas are combined to emulate a large-aperture antenna. The first integrated silicon-based phased array receiver, operating at 24 GHz, was demonstrated by Caltech researchers in 2004 [16]. Caltech researchers also demonstrated a CMOS 24-GHz phased array transmitter in 2005 [17] and a fully integrated 77-GHz phased array transceiver with integrated antennas in 2006 [18], [19].

The miniaturization of phased arrays has led to several sensing applications such as automotive radars for ADAS (resulting in road safety improvement) [20], [21], civil aircraft navigation, and ultrasound imaging systems (where phased arrays operate on sound waves rather than electromagnetic (EM) waves). Recently, phased arrays have been utilized for a broad range of commercial applications and are desired for a number of emerging applications some of which are described in this chapter.

1.2 Current and Emerging Applications of Phased Array Antennas

Phased arrays have been widely utilized in military radar applications for many decades. Fig. 1.2 shows some phased array applications in military radars. Recently, phased arrays have been utilized in radars for ADAS and autonomous vehicles. Automotive radar-based technologies can assist drivers in different ways such as providing sideway and forward collision warning, as shown in Fig. 1.3. They can also be combined with advanced systems like automatic emergency braking for collision avoidance.

Phased array antennas have also become a part of 5G communication systems. In 5G communications, it is desired to provide a high data rate, which calls for a large bandwidth (BW). It necessitates system operation at high frequencies where a large unlicensed spectrum is available,

(a)

(b)

Fig. 1.2. Phased array applications in (a) warplane and (b) battleship.

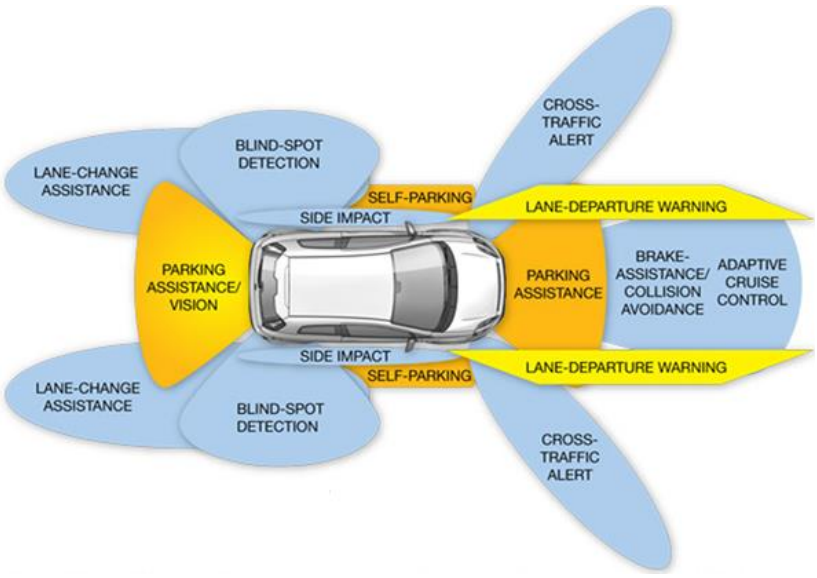


Fig. 1.3. Automotive radars in advanced driver assistance systems.

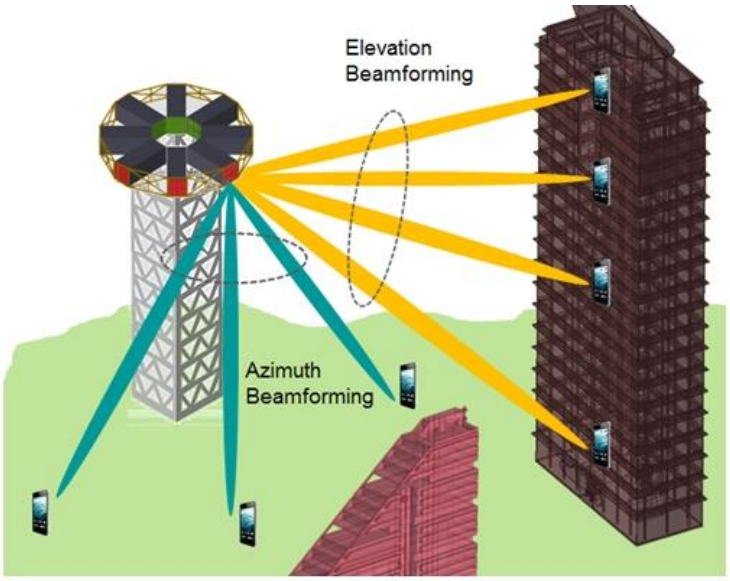


Fig. 1.4. Phased array application in a 5G communication network.

and it is feasible to provide a large bandwidth. However, due to the large free space path loss at high frequencies, signals will be severely attenuated while propagating. As a result, a large transmit power is required at high frequencies. Phased arrays with focused beam are utilized in 5G mobile terminals to relax the requirement of the transmit power. Phased arrays also increase the channel capacity and reduce multipath fading and co-channel interference in 5G communication systems. Fig. 1.4 shows phased array application in a 5G communication network.

Phased arrays are also highly attractive for radiative RF wireless power transfer (WPT) systems to enhance the power transfer range and efficiency in WPT applications including wireless sensor networks (for inter-vehicle and vehicle-to-infrastructure communication, etc.), micro-aerial-vehicles, internet of things (IoT), and space-based solar power transfer [22], as shown in Fig. 1.5.

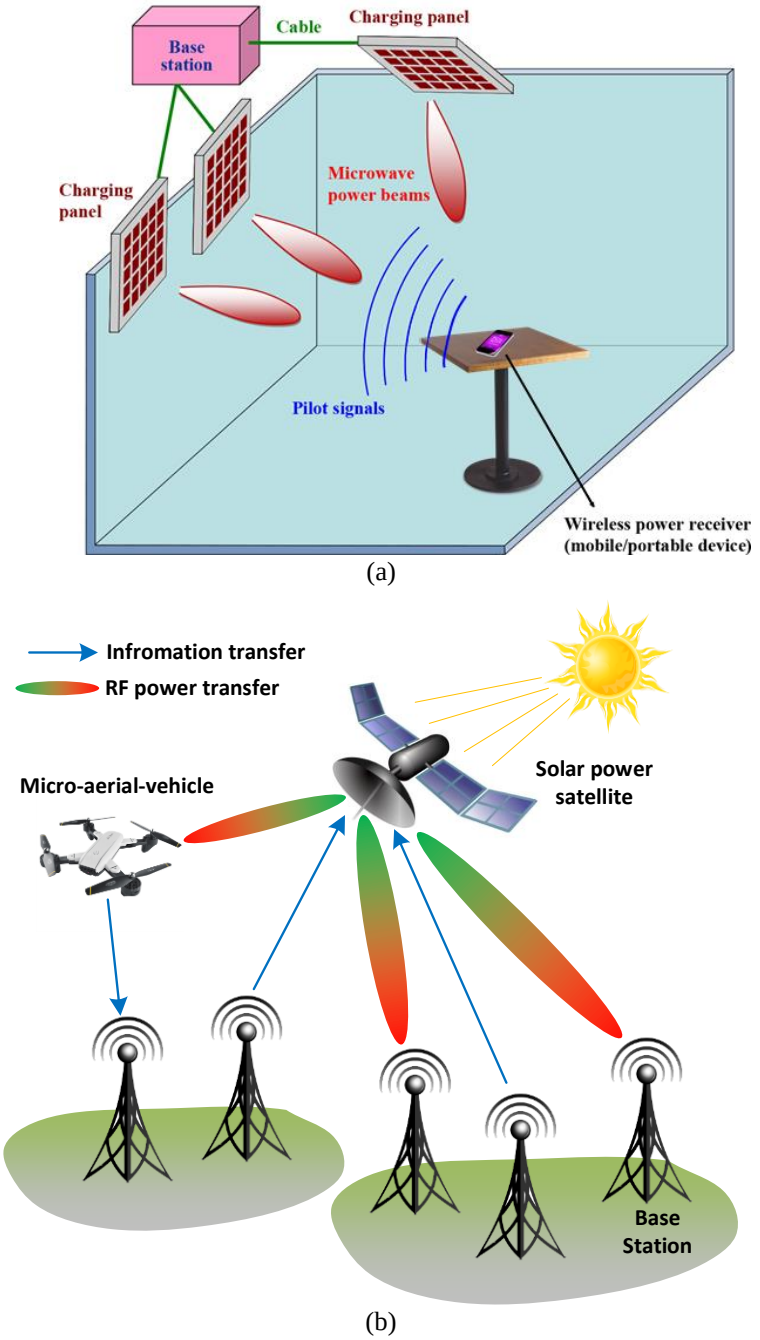


Fig. 1.5. Emerging phased array applications in wireless power transfer systems for charging (a) mobile portable devices and (b) mobile base stations and micro-aerial-vehicles.

1.3 Operation Principle of Phased Array Antennas

In the following, equations of a receive phased array are derived. The equations for a transmit phased array are the same as a receive phased array due to the reciprocity. The operation principle of a receive phased array is illustrated in Fig. 1.6. In an N-element linear array with identical antenna elements that are equally spaced by a distance of d, a plane-wave incident upon the array at an angle of θ (with respect to a direction normal to the array) arrives at the nth element after experiencing an excess delay τ_n given by Eq. 1.1

$$\tau_n = n\underbrace{\frac{dsin(\theta)}{c_0}}_{\tau}, \tag{1.1}$$

where c_0 is the speed of EM waves in free space. The plane wave experiences a linear delay progression as it arrives at the successive antenna elements across the array. In other words, the time delay τ_n is n times more than the time delay that the signal experiences in arriving at adjacent antennas, denoted by τ in Eq. 1.1. This delay progression can be reversed by adjusting the delays provided by the variable delay blocks in the phased array circuit. Assuming that the incident signal is a sinusoid with a frequency of ω and amplitude of A and assuming a linear phase progression by increments of φ for the variable delay circuits along the array, the output signal of the variable delay block in nth channel can be written as Eq. 1.2

$$S_i = Ae^{-j\omega\tau_n}e^{j\varphi_n} = Ae^{-j\omega n\tau}e^{jn\varphi}. \tag{1.2}$$

Subsequently, the array factor, which is equal to the summation of the signals at all channels normalized to the signal at one channel, can be written as Eq. 1.3

$$F = \sum_{n=1}^{N} e^{-jn(\omega\tau-\varphi)} = \frac{Sin^2\left({}^{N}/_{2}\left({}^{2\pi d}/_{\lambda}\sin(\theta)-\varphi\right)\right)}{Sin^2\left(\left({}^{2\pi d}/_{2\lambda}\sin(\theta)-\varphi\right)\right)}, \tag{1.3}$$

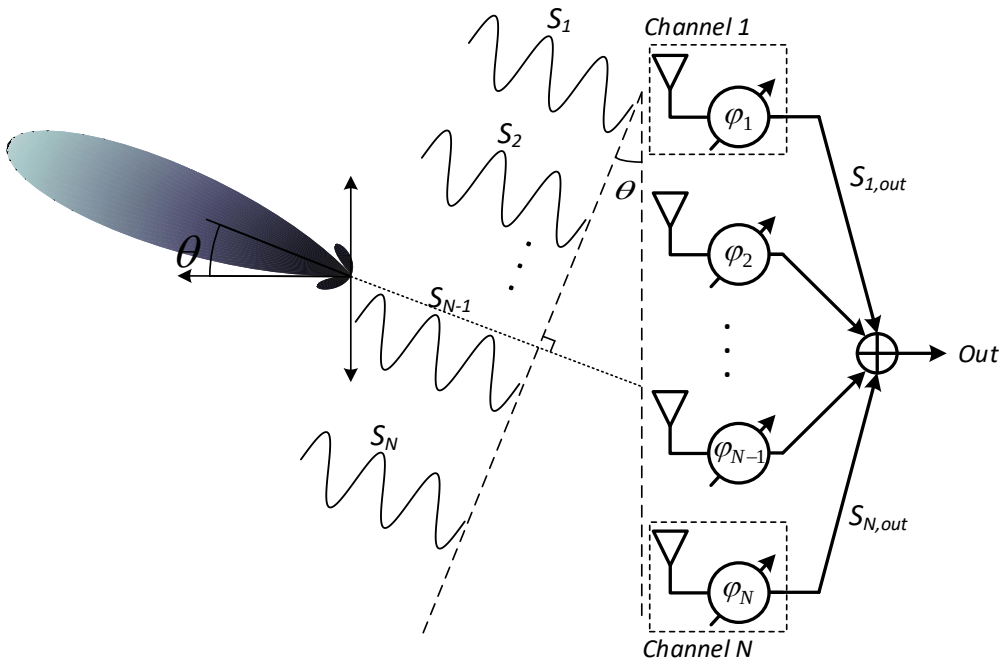


Fig. 1.6. Block diagram of an N-element linear phased array receiver.

where λ is the signal wavelength in free space. Based on Eq. 1.3, the peak of the array factor occurs at an incident angle given by Eq. 1.4

$$\theta = \sin^{-1}\left(\frac{\lambda}{2\pi d}\varphi\right). \tag{1.4}$$

At this angle, the time delays of the variable delay blocks compensate the linear delay progression experienced by the incident wave. As a result, the signals (at all channels) combined at the output of the receive array are coherent, and the array factor F obtains its maximum value. The incident angle θ, indicating the direction of the array factor's main lobe, is called scan angle. The array factor is equal to N^2 for θ and lower than N^2 for other incident angles, demonstrating spatial selectivity of phased arrays. The difference between the value of F at θ and other incident angles (selectivity) is a function of N, as shown in Fig. 1.7 that presents array factor at the scan angle of 0° (boresight) for four, eight, and sixteen element phased arrays. Phased arrays' selectivity and the maximum value of F, corresponding to the scan angle of θ, increase as the number of elements (N) increases.

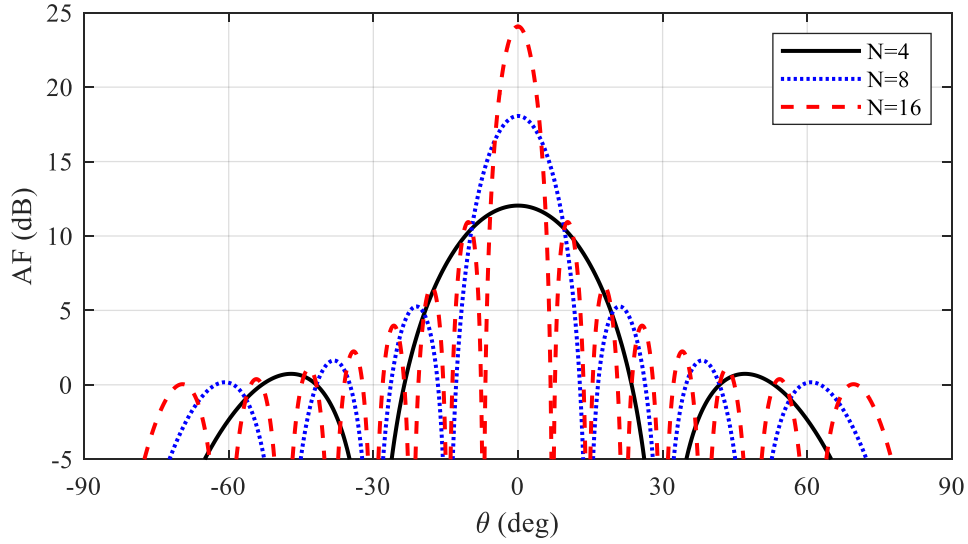


Fig. 1.7. Array factor at the scan angle of 0° for uniformly-excited linear phased arrays with different number of elements.

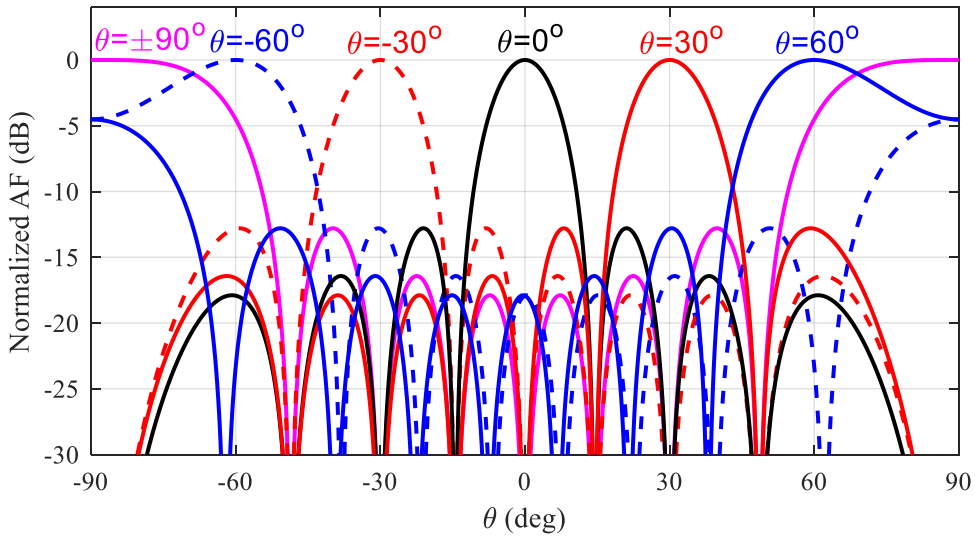


Fig. 1.8. Normalized array factor of an eight-element uniformly excited linear phased array at different scan angles.

In addition to spatial filtering (suppressing the signals coming from directions other than scan angle) and beamforming, phased arrays offer beam steering which is the capability of changing the direction of the main lobe. This can be achieved by electronically adjusting the variable delays in the channels. Fig. 1.8 shows the normalized array factor of an eight-element uniformly-excited phased array at different scan angles.

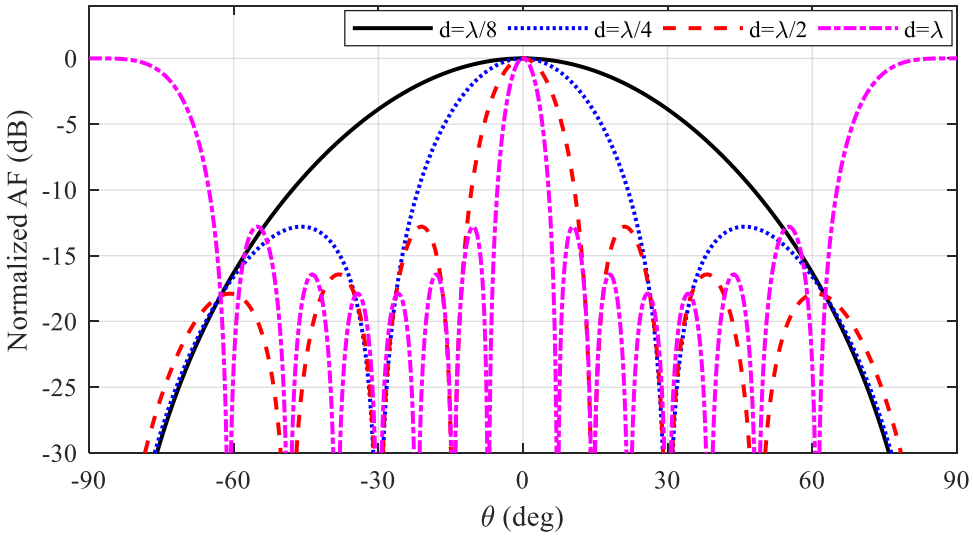


Fig. 1.9. Normalized array factor for an eight-element uniformly excited linear phased array with different antenna spacing.

Various array factors can be obtained by different configurations and excitations of the antennas in an N-element phased array.

The normalized array factor of an eight-element uniformly excited phased array with different inter-element spacings is shown in Fig. 1.9. According to the Fig. 1.9, increasing the inter-element spacing results in decreasing the beamwidth of the array. However, for inter-element spacings larger than $\lambda/2$, it will cause grating lobes to appear in the visible region.

One can also use non-uniform excitation (tapered excitation) for shaping the array factor (such as adjusting sidelobe levels or adjusting null positions at specific directions). The array factor of an eight-element linear phased array with several well-known tapered excitations are shown in Fig. 1.10. Dolph-Chebyshev excitation provides the same-level lobes (the level is adjustable) while binomial tapering eliminates all the lobes at the cost of the largest beamwidth compared to the uniform and Dolph-Chebyshev excitations. In practice, binomial tapering cannot be used for large-scale arrays since it requires a huge amplitude difference for the excitation signals across the array [23].

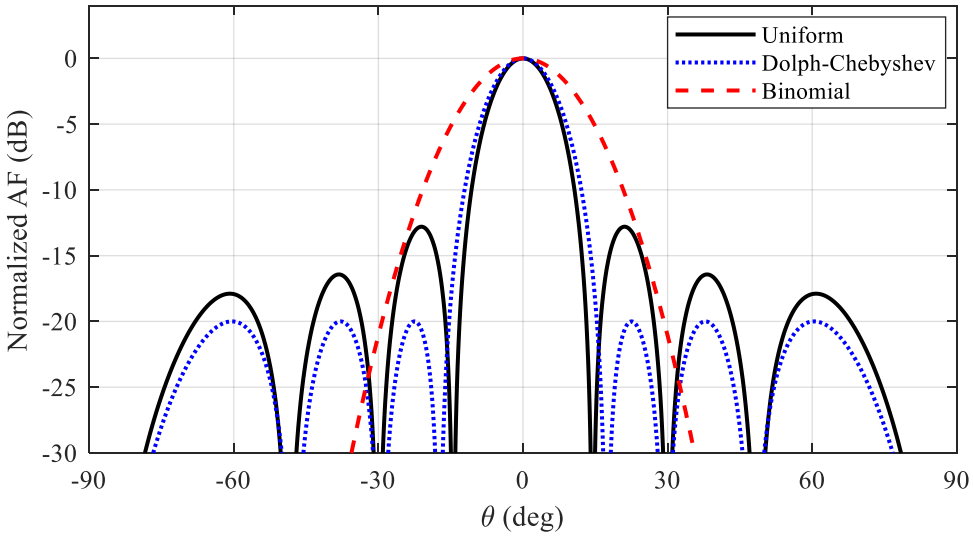


Fig. 1.10. Normalized array factor for an eight-element linear phased array with different tapered excitations.

In general, phased arrays provide beam forming and steering by adjusting the relative phase and amplitude of the excitation signals across the array elements.

The overall radiation pattern of an array of identical antennas is determined by the product of the array factor by the radiation pattern of each individual antenna.

1.4 Advantages of Phased Array Antennas

1.4.1 Reducing co-channel interference and multipath fading

Due to the beamforming offered by phased arrays, they can reduce co-channel interference and multipath fading in communication systems.

Co-channel radio interference is crosstalk between two radio transmitters using the same frequency. Co-channel interference is mitigated in phased array systems due to the high directivity of phased array transmitters and spatial filtering of phased array receivers.

In communication systems, a transmit signal travels through a number of different paths to reach the receiver. Therefore, the signals arrive at the receiver (emanated from the transmitter) come from a variety of paths (with different delays) and have different phases. These out-of-phase

signals are combined destructively thereby attenuating or canceling each other. This phenomenon is called multipath fading. Phased array systems can significantly reduce multipath fading due to their high directivity and spatial filtering.

1.4.2 Sensitivity enhancement in phased array receivers

Sensitivity in a receiver is defined as the minimum power of the input signal (S_{min}) which is required to produce a specified output signal with a specific signal-to-noise (SNR) ratio. Sensitivity is given by Eq. 1.5

$$S_{min} = SNR_{min} \times kT_0B \times \text{NF}, \tag{1.5}$$

where SNR_{min} is the minimum signal-to-noise ratio required at the output of the receiver to detect and process the transmitted signal, k is the Boltzmann's constant (= 1.38 ×10-23 J/K), T_0 (K) is the absolute temperature of the receiver input, B (Hz) is the receiver bandwidth, and NF is the noise factor of the receiver. In a phased array antenna that receives a signal coming from the scan angle direction, the signals at the outputs of the channels are added coherently. Assuming that the signals are combined in current domain, the signal power at the output of an N-element array is N^2 times larger than the signal power received by the individual antennas. On the other hand, the noise of the receiver channels will be added incoherently, thereby increasing the total noise power by a factor of N. Due to the coherent combination of the signals and incoherent combination of the noise in different channels (shown in Fig. 1.11), the noise factor and SNR of the entire system will be improved by a factor of N. Subsequently, the sensitivity of an N-element array will be N times larger than the sensitivity of a single channel. Noise factor and sensitivity of a phased array are given by Eq. 1.6 and Eq. 1.7, respectively.

$$NF_{array} = \frac{SNR_{in-array}}{SNR_{out-array}} = \frac{S_{in}}{N^2 S_{out}} \frac{N \times N_o}{N_{in}} = NF_{channel}/N \tag{1.6}$$

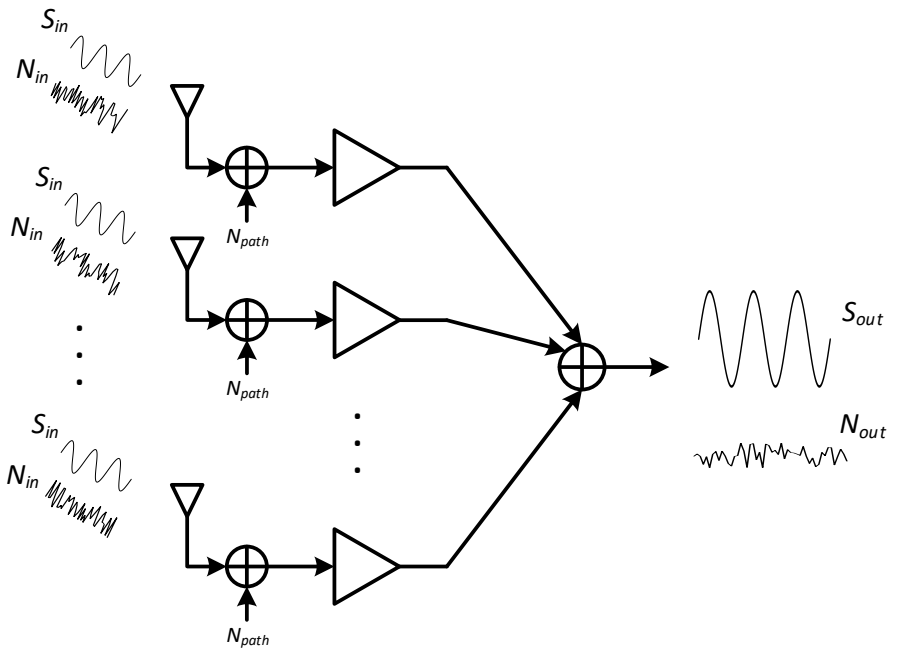


Fig. 1.11. Enhancement of NF and SNR in an N-element receive phased array.

$$Sensitivity_{array}\,(\text{dB}) = Sensitivity_{channel}\,(\text{dB}) + 10\log_{10}^{\text{N}}. \tag{1.7}$$

Due to their capability of improving SNR and sensitivity as well as reducing multipath fading and co-channel interference, phased arrays are highly attractive for current and emerging communication systems. Phased arrays can also improve SNR and cross-range resolution of radar systems, making them highly attractive for radar applications as well.

1.4.3 Increasing gain and EIRP in phased array transmitters

Phased array antennas can focus the transmitting signal toward a specific direction, thereby boosting the power level transmitted at that direction. As a result, phased arrays provide higher directivity and larger gain. Consequently, for a specific power level at the receiver, the required transmit power in communication systems using phased arrays will be reduced. From another point of view, phased arrays allow for longer communication distance given a specific power level at the transmitter and a specific required power at the receiver.

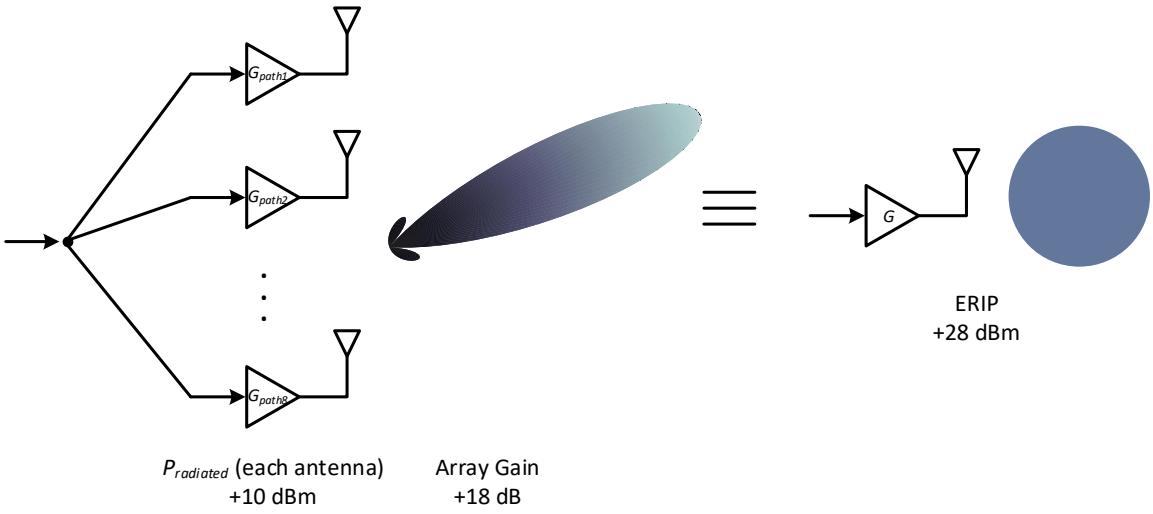


Fig. 1.12. EIRP enhancement in an eight-element phased array transmitter.

Effective (or equivalent) isotropic radiated power (EIRP) in a particular direction is a metric of the total power that would have to be radiated by a hypothetical isotropic antenna to generate the same signal power as the real source in the same direction. An N-element phased array increases effective EIRP in the direction of the main beam by a factor of N^2. Fig. 1.12 shows EIRP improvement in an eight-element phased array with 10 dBm output power at each radiating element.

1.5 Phased Array Architectures

In a phased array system, phase shifting can occur at each of the RF, LO, IF, or baseband stages. Phased array architectures have been conventionally categorized into four types: RF-phase shifting, LO-phase shifting, IF-phase shifting, and Digital phased arrays based on the stage at which phase shifting occurs. In this section, the aforementioned phased array architectures are discussed and compared with each other in receive mode. The architectures of phased array transmitters can also be divided into the same four categories.

General architectures of RF-phase shifting, LO-phase shifting, IF-phase shifting and digital phased array receivers are shown in Fig. 1.13, Fig. 1.14, Fig. 1.15, and, Fig. 1.16 respectively.

In an RF-phase shifting phased array receiver, the signals received by the antenna elements are phase shifted and combined in the RF domain. Subsequently, the signal is down converted to baseband using a heterodyne or homodyne mixing architecture. In a LO-phase shifting phased array receiver, the RF signals are mixed with the LO signals that have a specific relative phase across the array. The down converted signals are then combined in the IF domain. In an IF-phase shifting phased array receiver, the signals received by the antenna elements are down converted to

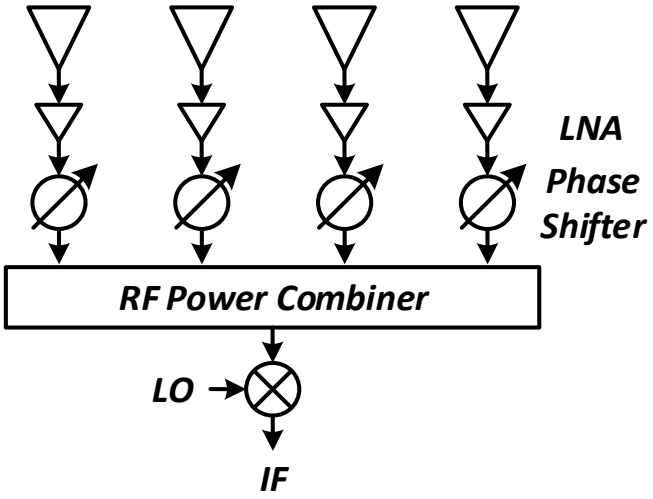


Fig. 1.13. Architecture of an RF-phase shifting phased array receiver.

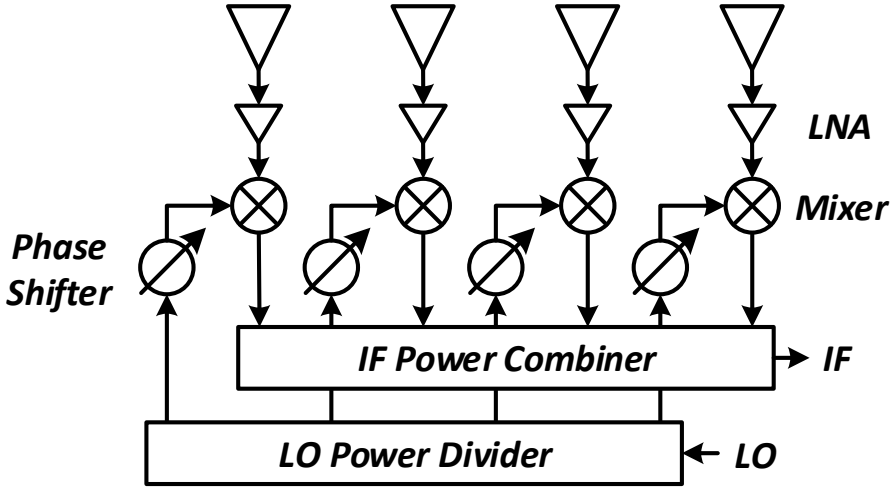


Fig. 1.14. Architecture of a LO-phase shifting phased array receiver.

IF, and the IF signals are then phase shifted and combined. In a digital phased array receiver, the down converted signal at each channel is digitized using an analog to digital converter. The digital signals are then processed using a digital signal processing unit (DSP) for beamforming purposes.

Each of the described phased array architectures has several advantages and disadvantages compared to one another. In an RF-phase shifting phased array receiver, where the signals are

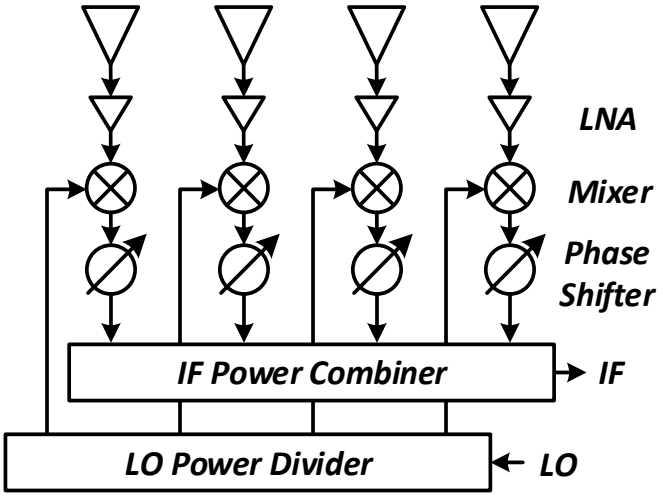


Fig. 1.15. Architecture of an IF-phase shifting phased array receiver.

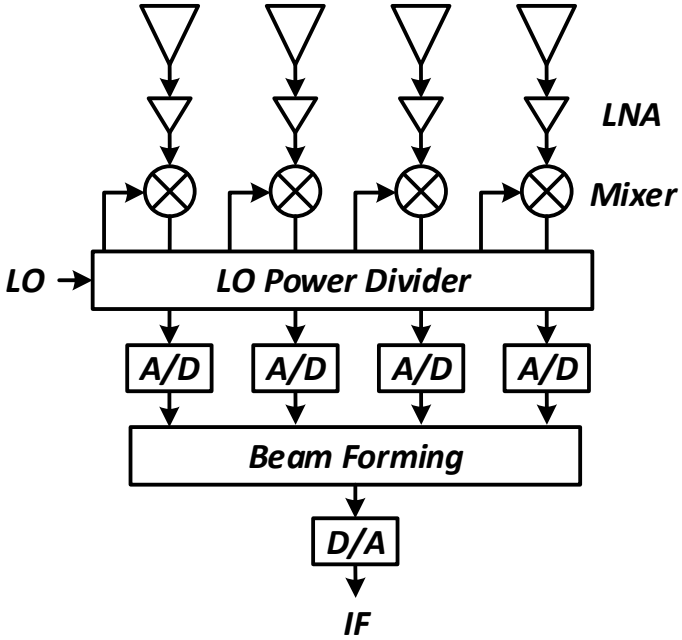


Fig. 1.16. Architecture of a digital phased array receiver.

phase shifted and combined in the RF stage, only one mixer is required to down convert the RF signal, and there is no need to distribute LO signals. Consequently, RF-phase shifting phased arrays are usually the most compact architecture compared to the other types. Furthermore, since the phase shifted signals are combined in the RF stage, thereby providing spatial filtering in the RF domain, a larger portion of the receiver chain is immune to the interferences coming from undesired directions. As a result, the linearity and dynamic range requirement of the down conversion mixer and its proceeding blocks is not as stringent as the requirements in the other types of phased array architectures.

The main challenge of RF-phase shifting architectures is that the phase shifters are required to operate with high performance at RF/mm-wave frequencies. However, conventional passive phase shifters operating at RF/mm-wave frequencies are too lossy, degrading NF in a receiver and efficiency in a transmitter. Active RF/mm-wave phase shifters also suffer from a limited dynamic range.

Another important challenge of this architecture is that the employed phase shifters should exhibit a nearly constant loss/gain over the entire phase tuning range. The reason is that the loss/gain of these phase shifters directly impacts the gain of the chain and any variation in phase shifters' loss/gain over the phase tuning range varies the gain of the chain versus scan angle. Maintaining the loss/gain of the RF/mm-wave phase shifters over the entire phase tuning range is challenging.

On the other hand, the phase shifters in the LO-phase shifting phased arrays are not placed in the signal path and, consequently, their specifications such as loss, noise contribution, linearity, and output amplitude variation over the phase tuning range minimally impact the overall system performance. This is considered as one of the advantages of LO-phase shifting architectures.

However, this architecture requires a larger number of mixers compared to RF-phase shifting phased arrays. Therefore, their overall complexity, size, and power consumption will be potentially higher than the RF-phase shifting phased arrays.

In the IF-phase shifting phased arrays also, phase shifters are placed in the signal path and their performance directly impacts the overall performance of the array. However, since phase shifting is performed at much lower frequencies than RF, phase shifters can be designed with much better performance in terms of loss, NF, linearity, and consistency of the output amplitude over the phase tuning range. As a drawback of this architecture, similar to LO-phase shifting phased arrays, a larger number of mixers is required in the system, which can add to the overall size, system complexity and power consumption.

Digital phased arrays are featured by their flexible functionality. They can create multiple beams and offer multiple input, multiple outputs (MIMO). They can also adaptively update their pattern and process data using various complex signal-processing algorithms. However, like the LO and IF-phase shifting phased arrays, each channel requires all the blocks of an RF chain front-end, resulting in an overall complexity, large size, and high power consumption. It should also be noted that, in this architecture, the interference is not cancelled out until after signal processing. Therefore, the entire receiver blocks have strict linearity requirements.

1.6 Phased Arrays' Challenges

Despite numerous applications of phased arrays, there are still some challenges regarding their complexity, size, and cost that need to be addressed.

Among the described phased array configurations with different advantages and challenges, there is one common feature which is utilizing one phase shifter per each antenna element. Phase

shifters and their associated control circuitry are responsible for a large portion of complexity and size of conventional phased arrays.

Ongoing attempts have been made to develop new architectures for reducing phased arrays' complexity and size, some of which are discussed in the following section.

1.7 Review of the State-of-the-Art Phased Arrays with Reduced Complexity

In conventional phased arrays, to adjust the signal phase across the array elements, one tunable phase shifter is used at each array element. Phase shifters and their control circuitry play a significant role in determining the complexity and size of conventional phased arrays.

A number of publications on phased array design have discussed architectures that can reduce the complexity of phased arrays either by reducing the number of phase shifters [24] – [28] or integrating the phase shifting function into the array feed network [29], [30]. A commonly used approach to reduce the number of phase shifters is based on grouping the radiating elements into a number of uniform subarrays, where each subarray is fed by a single phase shifter [24]. The array factor for such a phased array is equal to the product of two independent array factors, one related to a subarray (primary array) and the other corresponding to the group of subarrays (secondary array). The spacing between the adjacent elements (inter-element spacing) of the secondary array is proportional to the number of elements and inter-element spacing of the primary array. In such architectures, as the size of subarrays is increased, the grating lobes can appear in the visible region since the inter-element spacing of the secondary array increases. An alternative approach to remedy this problem is to use overlapping subarrays [25] – [27]. However, multiple crossovers used in the feed network of the overlapping subarrays hinder their planar implementation [28]. In another approach, phased array elements are grouped into a random combination of non-uniform

subarrays each being fed by a single phase shifter [28]. An algorithm is used to optimize the number of elements in each subarray, so that for a given number of array elements and a total number of phase shifters, the phased array provides the maximum scan range while the grating lobes are limited to a specified value. However, in such approaches, increasing the size of the subarrays can still cause the grating lobes to appear in the visible region unless the scan range is very limited.

The array presented in [29] integrates the phase shifting function into the feed network by utilizing a resonance power dividing circuit which performs both the power division and phase shifting functions. Consequently, the requirement of using separate power splitter and phase shifters in conventional phased arrays is eliminated. However, utilizing resonance power dividing circuits for the design of integrated phased arrays operating below Ka-band requires a large chip area since the operation of resonance power dividing circuits relies on quarter-wave transmission lines.

An integrated variable-phase ring oscillator and a phase locked loop architecture are used in [30] to eliminate phase shifters. However, the architectures presented in [30] do not simply support amplitude-modulation schemes such as QAM.

1.8 Thesis Overview

In this thesis, two new architectures for phased arrays with reduced number of phase shifters, less complexity, and small size are presented. In these architectures, phase-shifting function is integrated into new RF feed networks through vector-summation. The low-complexity architectures presented in this thesis can be utilized for designing phased arrays in receive as well as transmit mode. The integrated phased arrays, designed based on these architectures, can be

utilized in commercial applications such as 5G communications and automotive radars for ADAS and autonomous vehicles.

Moreover, two new integrated phase shifters with low power consumption, small size, and simple control are presented for further reduction of phased arrays' size and complexity.

This thesis is organized as follows. The new integrated phase shifters with small size and simple control are presented in Chapters 2 and 3. Chapter 2 describes a new CMOS vector modulator phase shifter operating based on the summation of rotating orthogonal vectors, and Chapter 3 presents a frequency tunable 360° analog CMOS phase shifter with an adjustable output amplitude.

A scalable limited-scan phased array with significantly reduced number of phase shifters and control signals operating at Ku-band is described in Chapter 4. A low-complexity, wide-scan, scalable, integrated phased array operating at K-band is presented in Chapter 5., followed by the conclusion and future works in Chapter 6.

Chapter 2: A Vector Modulator Phase Shifter Operating Based on the Summation of Rotating Orthogonal Vectors

2.1 Introduction

Phase shifters are one of the key components of phased array antennas and are responsible for adjusting the phase of the signals transmitted or received by the antenna elements. Phase shifters and their control circuitry also play a major role in determining the complexity, size, and cost of phased arrays [31]. Active vector modulator phase shifters can provide 360° of phase tuning while occupying a small area [32] – [36] and have been utilized in the design of integrated phased arrays [37] – [41].

The principle of operation for a conventional vector sum phase shifter is illustrated in Fig. 2.1. The input signal is divided into quadrature signals (vectors), I and Q, whose amplitudes are adjusted using variable gain amplifiers. Subsequently, the weighted orthogonal vectors are added to generate a vector-sum signal (denoted by S) with a tunable phase. To preserve the vector sum magnitude while tuning its phase, the amplitudes of both the I and Q vectors should be adjusted.

In this chapter, a new circuit topology for a vector modulator phase shifter is introduced. In this circuit, phase shifting is achieved through simultaneous variation of both the amplitude ratio and phases of I and Q signals, while keeping the relative phase between I and Q constant, as shown in Fig. 2.2 [42]. Simultaneous phase and amplitude ratio variation of I and Q vectors are obtained by adjusting the value of a single pair of identical variable capacitors in the circuit. Equal phase variation (rotation) of I and Q vectors varies the phase of the vector sum signal while maintaining

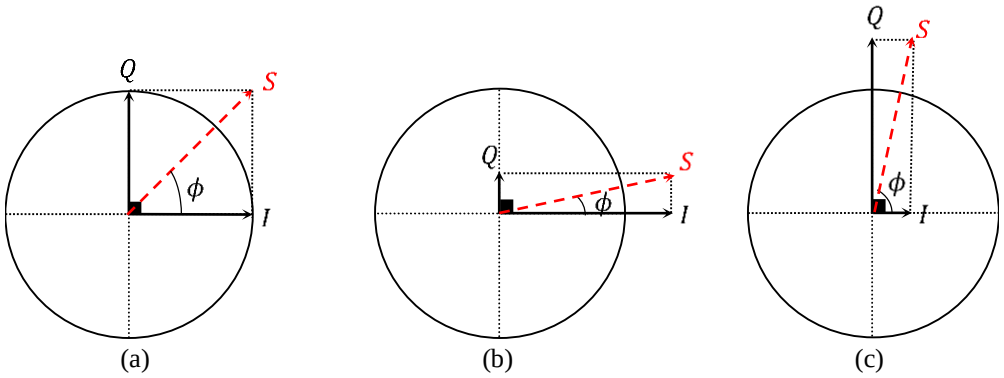


Fig. 2.1. Principle of operation for a conventional vector modulator phase shifter. (a) Vector sum phase = 45°. (b) Conditions for decreasing and (c) increasing the vector sum phase by varying the amplitudes of I and Q vectors.

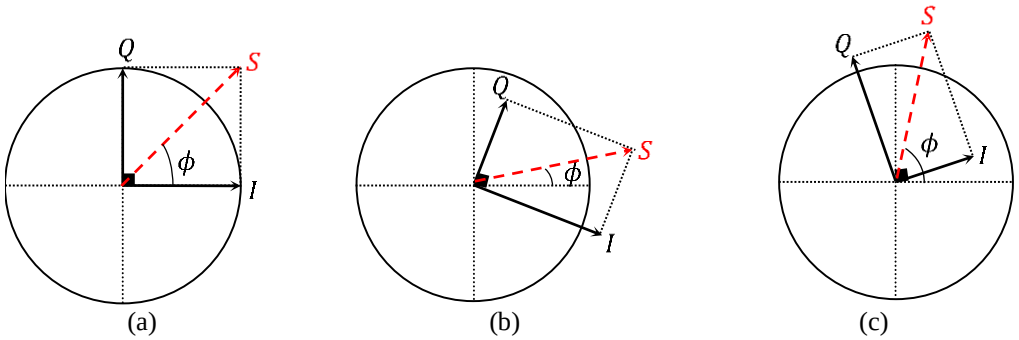


Fig. 2.2. Principle of operation for the phase shifter in this work. (a) Vector sum phase = 45°. (b) Conditions for decreasing and (c) increasing the vector sum phase by simultaneously varying the amplitudes and phases of I and Q vectors.

its magnitude. Therefore, the proposed vector modulator phase shifter allows for tuning the vector sum phase with minimum vector sum magnitude variation over the phase tuning range.

This chapter introduces the circuit architecture of the proposed vector modulator phase shifter operating based on the summation of rotating orthogonal vectors and provides a detailed analysis of the circuit. It also provides an optimum design for maximum phase tuning range with a constant output amplitude. Furthermore, the simulation results showing the performance of a single-stage CMOS vector modulator phase shifter designed at K-band for maximum phase tuning range with a nearly constant output signal amplitude are presented.

According to the theoretical analysis, the maximum achievable phase tuning range with a constant output amplitude is only a function of the tuning range of the identical varactors in the circuit. In theory, the phase shifter can provide up to 180º of phase variation with a constant output

amplitude assuming that the varactors could provide a very large tuning range. However, in practice, the tuning range of the varactors is limited by the fabrication technology, which constrains the maximum phase tuning range for the phase shifter with a constant output amplitude. To increase the maximum achievable phase tuning range, while keeping the magnitude variation relatively small, multiple switched varactors are employed in the phase shifter core to increase the overall tuning range of the variable capacitors. This technique allows for both coarse and fine tuning of the phase and does not add to the overall power consumption and chip area.

The vector modulator phase shifter introduced and analyzed in this chapter is a fully differential circuit that can be utilized by itself in an integrated phased array with differential signaling. In this work, however, it is connected to an active balun at the input and a buffer at the output, which also provide input and output matching, to allow for the phase shifter operation as a stand-alone integrated circuit (IC) with single-ended input and differential outputs. The stand-alone integrated phase shifter is designed and fabricated at K-band in 130-nm CMOS process. It provides more than 290° of continuous phase tuning over the band 21−24 GHz while occupying an area of 0.64×0.68 mm^2 (excluding the pads) and consuming 18.5 mW of dc power. The phase shifter core consumes only 7.8 mW of power, and its corresponding area is 0.15×0.3 mm^2. Due to the integrated phase shifter's continuous phase tuning, compact size, and low power consumption, it is a promising candidate for integrated phased array systems such as automotive radars.

This chapter is organized as follows. A detailed analysis of the proposed vector modulator circuit, which is the basis of the phase shifter core in the fabricated IC, is presented in Section 2.2. The fabricated single-ended input, differential output phase shifter is described in Section 2.3. The simulation and measurement results are provided in Section 2.4, followed by the conclusion in Section 2.5.

2.2 Single-Stage Vector Modulator Circuit Analysis

2.2.1 Operation Principle of the Vector Modulator Phase Shifter with Rotating Orthogonal Vectors

The simplified circuit model for the proposed vector modulator phase shifter is shown in Fig. 2.3. The input signals are the differential currents i^+ and i^- with the same magnitude and 180° phase difference. The signals i_1^+, i_1^-, i_2^+, and i_2^- are given by Eq. 2.1 and Eq. 2.2

$$i_1^+ = -i_1^- = \frac{(-2L_PCs^2 - RCs)i^+}{s^3(RCL_PC_P) + s^2L_P(C_P + 4C) + sR(C + C_P) + 1} \tag{2.1}$$

$$i_2^+ = -i_2^- = \frac{(2L_PCs^2 + 1)i^+}{s^3(RCL_PC_P) + s^2L_P(C_P + 4C) + sR(C + C_P) + 1}, \tag{2.2}$$

where $s = j\omega$. The currents i_1^+ and i_1^- as well as i_2^+ and i_2^- are equal in magnitude but 180° out of phase. The current signal i_1^+ is added to i_2^+ while i_1^- is added to i_2^-, generating differential current

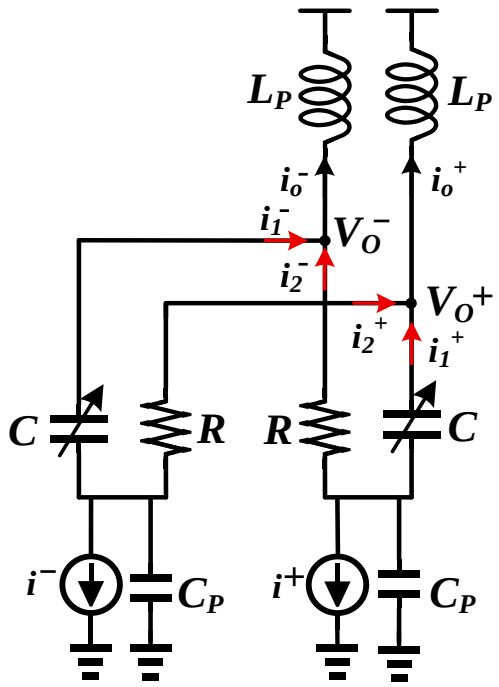


Fig. 2.3. Simplified ac-model for the proposed vector modulator phase shifter

signals i_o^+ (= $i_1^+ + i_2^+$) and i_o^- (= $-i_o^+$) that flow into the output load, L_p. The output current signal i_o^+, given by Eq. 2.3

$$i_o^+ = i^+ \underbrace{\frac{1}{s^3(RCL_PC_P) + s^2L_P(C_P + 4C) + sR(C + C_P) + 1}}_{Q}$$

$$+i^+ \underbrace{\frac{-RCs}{s^3(RCL_PC_P) + s^2L_P(C_P + 4C) + sR(C + C_P) + 1}}_{I}, \tag{2.3}$$

is equal to the summation of two orthogonal vectors, I and Q, where Q leads I by 90°. The differential output voltage V_O (= $V_O^+ - V_O^-$) is given by Eq. 2.4

$$V_O = L_P s(i_o^+ - i_o^-) = L_P s(Q + I)(i^+ - i^-). \tag{2.4}$$

By increasing (or decreasing) the value of the varactor C, phases of the I and Q vectors equally decrease (or increase). At the same time, the amplitude ratio of the two vectors ($|I/Q|$), which is equal to $RC\omega$, increases (or decreases). Considering the variation trend of the amplitude ratio and phases of I and Q vectors as a function of C, the phase of V_O is a decreasing function of C, and as a result, the phase tuning range is given by Eq. 2.5

$$\Delta(\measuredangle V_O) = \measuredangle V_O|_{C_{min}} - \measuredangle V_O|_{C_{max}}. \tag{2.5}$$

2.2.2 Design of the Vector Modulator Phase Shifter for Maximum Phase Tuning Range with a Constant Output Amplitude

To preserve the output signal amplitude ($|V_O|$) over the phase tuning range, the following relation must be satisfied

$$L_P = \frac{C_P R^2}{4}. \tag{2.6}$$

Eq. 2.6 is derived by setting the derivative of $|V_O|$ with respect to C to zero. Satisfying Eq. 2.6,

which is independent of ω, guarantees a constant output amplitude over the phase tuning range at each of the frequency points within the phase shifter bandwidth. Subsequently, the phase variation range and the amplitude of the output signal as a function of frequency are given by Eq. 2.7 and Eq. 2.8, respectively:

$$\Delta(\measuredangle V_O) = tan^{-1}\left(\frac{2RC_{min}\omega(K_c-1)(K_c(RC_{min}\omega)^2+1)}{({K_c}^2(RC_{min}\omega)^4+1)-({K_c}^2-4K_c+1)(RC_{min}\omega)^2}\right) \tag{2.7}$$

$$|V_O| = |i^+ - i^-|\frac{R^2C_P\omega}{(RC_P\omega)^2+4}, \tag{2.8}$$

where K_c represents the varactor tunability and is equal to C_{max}/C_{min}.

The phase tuning range in Eq. 2.7 is a function of R, C_{min}, ω, and K_c. For a given K_c, in order to maximize the phase tuning range at the design frequency of ω_0, the following condition should be satisfied:

$$RC_{min}\omega_0 = \frac{1}{\sqrt{K_c}}\,. \tag{2.9}$$

Eq. 2.9 is derived by setting the derivative of Eq. 2.7 with respect to R (or C_{min}) to zero at ω_0. For the circuit satisfying both Eq. 2.6 and Eq. 2.9, the maximum achievable phase tuning range at the design frequency of ω_0 is equal to:

$$\Delta(\measuredangle V_O)|_{\omega_0} = 2\left(tan^{-1}\left(\sqrt{K_c}\right) - tan^{-1}\left(\frac{1}{\sqrt{K_c}}\right)\right). \tag{2.10}$$

According to Eq. 2.10, the phase shifter can theoretically provide up to 180º of phase tuning with a constant output signal amplitude at ω_0 given a varactor with a very large K_c. However, in practice, K_c is limited by the fabrication technology.

The output signal amplitude in Eq. 2.8 is an increasing function of R. For a given R, the output

signal amplitude at ω_0 will be maximized if:

$$C_P \omega_0 = \frac{2}{R} . \tag{2.11}$$

Eq. 2.11 is derived by setting the derivative of Eq. 2.8 with respect to C_P to zero at ω_0. For the circuit satisfying both Eq. 2.6 and Eq. 2.11, the maximum value of $|V_O|$ (at ω_0) that is maintained over the phase tuning range is given by Eq. 2.12

$$|V_O| = |i^+ - i^-| \, R/4 . \tag{2.12}$$

Based on the above analysis, to maximize phase tuning range and output signal amplitude at ω_0, while maintaining the amplitude over the phase tuning range, Eq. 2.6, Eq. 2.9, and Eq. 2.11 should be satisfied simultaneously.

For the circuit satisfying the criteria mentioned in Eq. 2.6, Eq. 2.9, and Eq. 2.11, the phase tuning range and amplitude of the output signal as a function of frequency are given by Eq. 2.13 and Eq. 2.14, respectively:

$$\Delta(\measuredangle V_O) = 2\left(tan^{-1}\left(\sqrt{K_c}\frac{\omega}{\omega_0}\right) - tan^{-1}\left(\frac{1}{\sqrt{K_c}}\frac{\omega}{\omega_0}\right)\right) \tag{2.13}$$

$$|V_O| = |i^+ - i^-| \frac{R\left(\frac{\omega}{\omega_0}\right)}{2\left(\left(\frac{\omega}{\omega_0}\right)^2 + 1\right)}. \tag{2.14}$$

At the frequency of ω_0, Eq. 2.13 and Eq. 2.14 are equal to Eq. 2.10 and Eq. 2.12, respectively.

It is noteworthy that in the circuit of Fig. 2.3 which is designed to satisfy Eq. 2.6, Eq. 2.9, and Eq. 2.11, half of the phase tuning range for the vector sum signal comes from the rotation of I and Q vectors while the other half is resulted by the variation in the amplitudes of I and Q (proof in Appendix 1).

It should be noted that Eqs. (2.1) – (2.14) are derived for the vector modulator circuit shown in Fig. 2.2 where the output loads are inductive. In practice, the phase shifter is followed by other blocks such as combiner/dividers in an integrated phased array system, and the proceeding CMOS stage will load the vector modulator circuit by its input capacitance. Considering the loading effect on the proposed vector modulator circuit, the required condition to preserve the output signal amplitude ($|V_O|$) over the phase tuning range at ω_0 is given by Eq. (2.15)

$$L_P\omega_0 = \frac{C_P\omega_0 R^2}{4 + C_P C_L {\omega_0}^2 R^2}, \tag{2.15}$$

where C_L is the loading capacitor. For the circuit satisfying Eq. (2.15), the required condition for maximizing phase tuning range and the corresponding maximum phase tuning range at ω_0 follow Eq. (2.9) and (2.10), respectively. The required condition for maximum output amplitude and the corresponding maximum output amplitude ω_0 also follow Eqs. (2.11) and (2.12), respectively.

2.2.3 Design of the Single-Stage Vector Modulator Phase Shifter Using 130-nm CMOS Process

A CMOS circuit topology realizing the introduced vector modulator phase shifter is shown in Fig. 2.4. The transistors M_1–M_4 form a differential cascode g_m-cell (with a simplified model shown in Fig. 2.3) generating differential current signals i^+ and i^-. The variable capacitors are realized by nMOS varactors with K_c of approximately 5 (available in the utilized technology) and are tuned by a single control voltage, V_{ctrl}. To decouple V_{ctrl} from the RF signal, a large resistor (R_B) is connected in series with the control voltage. The capacitors C_B are used to decouple the dc and RF signals.

To set the design parameters in the circuit of Fig. 2.4 for maximum phase tuning range at ω_0 while maximizing and maintaining the output amplitude, one can first determine the value of *R*. Then, the values of C_{min} and C_P can be calculated based on Eqs. 2.9 and 2.11, respectively. Subsequently, the value of L_P can be calculated using Eq. 2.6. To determine the value of *R*, one should first decide about the output amplitude (given by Eq. 2.12), overdrive voltage of the transistors $M_1 - M_4$, and gate-drain voltage of the transistors M_3 and M_4 which impacts their voltage headroom. The output amplitude, given by Eq. 2.12, is proportional to *R* and $(i^+ - i^-)$ which is a function of the transconductance of the transistors M_1 and M_2 (g_{m1} and g_{m2}). The values of g_{m1} and g_{m2} are determined by the size and bias current of M_1 and M_2 which should be the same size and equally biased to generate balanced signals $i^+$and i^-. The voltage drop across *R*, which is a function of the bias current of the transistors and the value of *R*, sets the gate-drain voltage of the identical transistors M_3 and M_4 and determines their headroom voltage. The overdrive voltage of M_1 and M_2 as well as M_3 and M_4 are also functions of the size and bias currents of the transistors. In general, the bias current and size of $M_1 - M_4$ as well as the value of *R* can be calculated assuming a specific output signal amplitude (for a given input signal), gate-drain voltage for M_3 and M_4 and overdrive voltage for $M_1 - M_4$. The rest of the design parameters can be subsequently calculated using Eqs. 2.6, 2.9, and 2.11.

Table 2.1. Design parameters

$(W/L)_{M1,\,M2}$ = 78 μm/0.12 μm	$(W/L)_{M3,\,M4}$ = 120 μm/0.12 μm
R = 115.5 Ω	R_B = 10.7 kΩ
C_{var1} = 31.9−160.9 fF	C_B = 5.2 pF
V_{DD} = 1.2 V	V_{ctrl} = 0−1.5 V
I_{Bias} = 4.5 mA	L_d = 510 pH

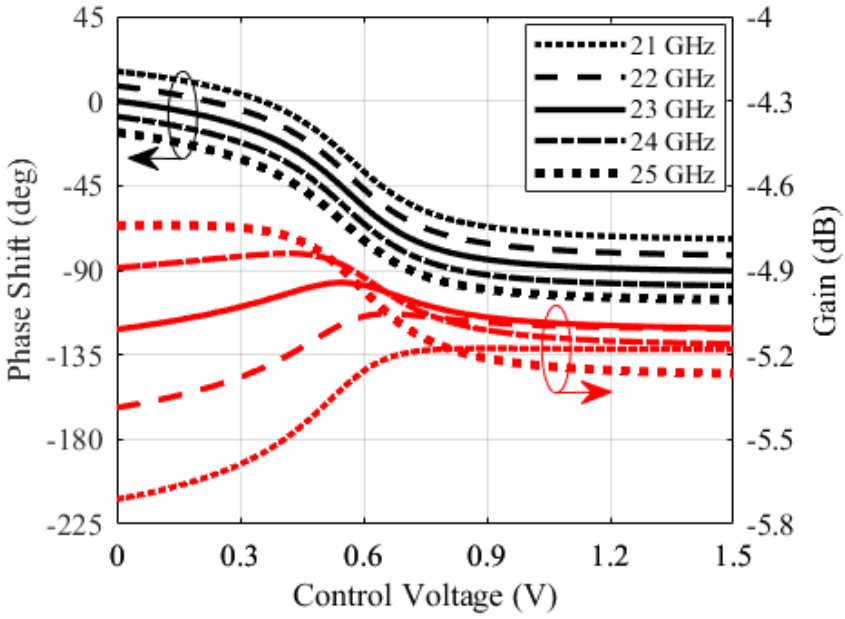


Fig. 2.5. Simulated differential phase and voltage gain of the 90° phase shifter, designed in 130-nm CMOS process, at different frequencies.

For the 130-nm CMOS phase shifter in Fig. 2.4, the phase tuning range predicted by Eq. 2.10 is 83.6° (obtained for K_c = 5). By optimizing the values of the circuit parameters, a phase variation range of 90° with a negligible output amplitude variation (less than 0.2 dB) over the phase tuning range at 23 GHz is obtained. The values for the circuit parameters in Fig. 2.4 are listed in Table 2.1. In this design, the capacitors C_P are realized by the parasitic capacitors of M_3, M_4, and nMOS varactors. Cadence Spectre simulation results showing the differential phase and voltage gain of the circuit in Fig. 2.4 as a function of the control voltage are presented in Fig. 2.5. According to the results, the phase tuning range is 90° with less than 1° variation within the range 21−25 GHz. The gain varies less than 1 dB over the entire phase tuning range and the specified band.

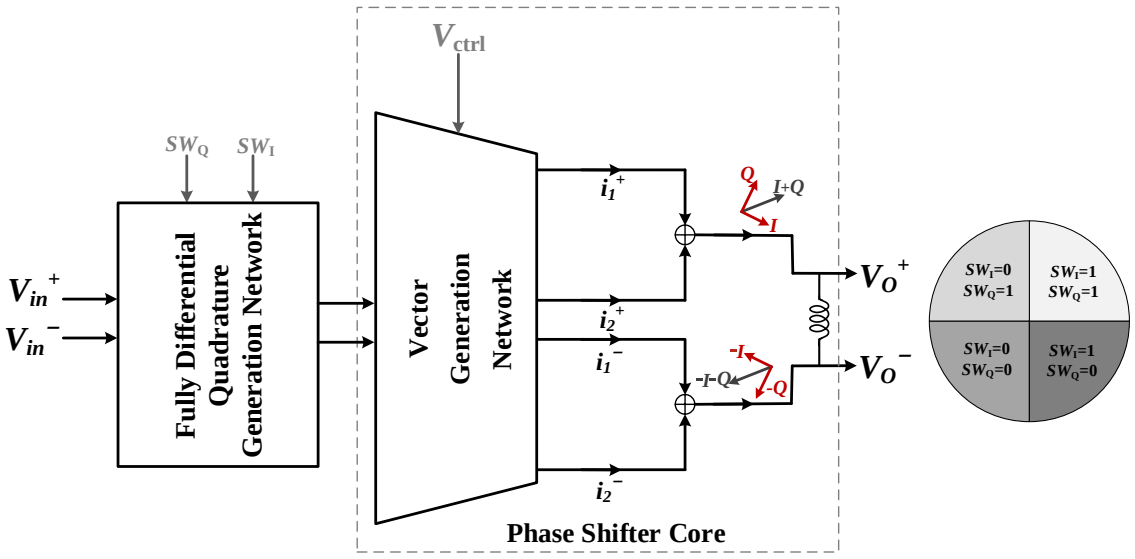


Fig. 2.6. Block diagram of a vector sum phase shifter employing the proposed phase shifter core, providing 360° of continuous phase tuning with a constant output amplitude by adjusting a single analog and two digital controls.

To expand the phase tuning range to 360° while maintaining the output signal amplitude, i^+ and i^- can be generated using a fully differential quadrature generation network [43], [44] with quadrant selector switches to allow for coarse phase variation of i^+ and i^- by increments of 90° (0°, 90°, 180°, and 270°), as shown in Fig. 2.6.

In this work, rather than using a differential quadrature generation network, multiple switched varactors are employed in the vector modulator circuit to expand the phase tuning range (through increasing the overall tuning range of the variable capacitors) while preserving the power consumption and chip area.

To realize a stand-alone integrated phase shifter with a single-ended input and differential outputs, the vector modulator circuit employing multiple switched varactors is connected to an active balun at the input and a buffer at the output that also serve as input and output matching networks, respectively. The stand-alone IC, which is designed at K-band and fabricated in 130-nm CMOS process, provides 300° of continuous phase tuning for each of the differential outputs (with 180° phase difference between the outputs). It is possible to obtain any phase shift within a range of 360° by selecting the polarity of the differential output signals.

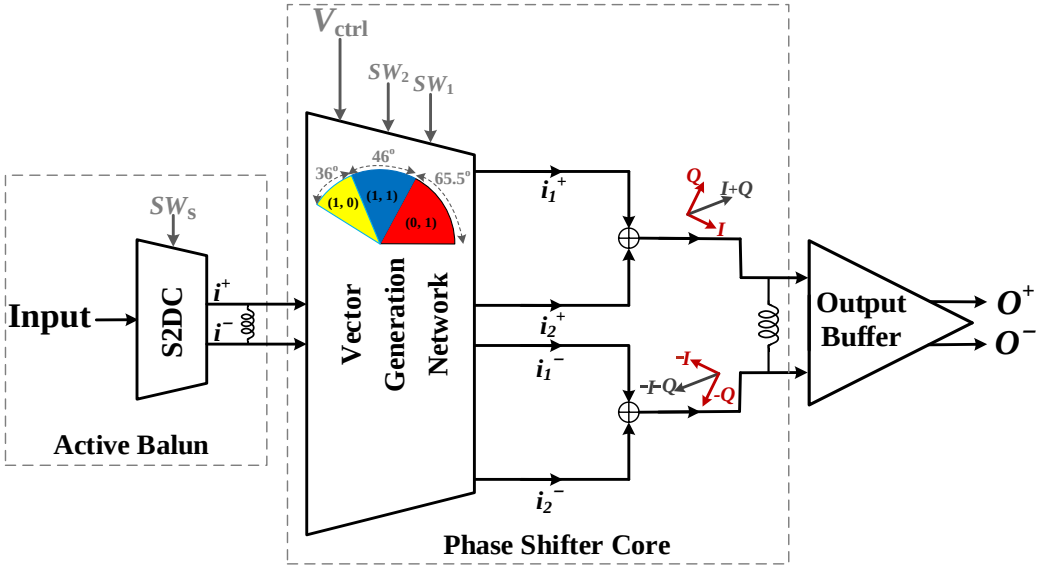


Fig. 2.7. Block diagram of the fabricated phase shifter. The phase tuning range for different switching states (SW_2, SW_1) with reference to the phase at (SW_2, SW_1) = (0, 1) and V_{ctrl} = 1.5 V are highlighted with three different colors.

2.3 A Phase Shifter with a Single-Ended Input and Differential Outputs

The block diagram of the fabricated phase shifter is shown in Fig. 2.7. The first stage is an active balun which also serves as the input matching network. It consists of a single-ended to differential signal converter (S2DC) in conjunction with a switch (SW_S) selecting the polarity of the S2DC's output differential signals. The second stage is the phase shifter core that performs all the tasks of vector generation, vectors' amplitude and phase variation, and vector summation to generate a signal with a tunable phase. The phase shifter core employs multiple switched varactors that are controlled by one analog and two digital inputs. The variable capacitors are switched by SW_1 and SW_2 (allowing for coarse tuning of the phase), and their capacitances are continuously varied by tuning V_{ctrl} (allowing for fine tuning of the phase). The output stage is a buffer that also provides output matching.

The circuit diagrams for the three stages of the fabricated phase shifter (input active balun, phase shifter core, and output buffer) are shown in Fig. 2.8. The active balun, shown in Fig. 2.8(a),

is formed by a common-gate stage in parallel with a common-source stage [45]. This stage amplifies the single-ended input signal and generates differential output signals V_O^+ and V_O^- while contributing to match the input impedance to 50 Ω. The inductor L_M is also used to resonate with the capacitive part of the input impedance to allow for input matching. The capacitors C_{CG} and C_{CS} and the large resistor R_B are used for decoupling dc and RF signals.

The cascode switched transistor pairs (M_{p1}, M_{p2}) and (M_{n1}, M_{n2}), controlled by complementary signals SW_s and $\overline{SW}_s$, are used to reverse the current flow direction through L_{P1} when the logic state of SW_s is inverted. This results in 180° of phase shift for the balun's output signals given the same size for (M_{p1}, M_{p2}) and (M_{n1}, M_{n2}). However, it is possible to generate a phase shift value other than 180° by changing the relative size of (M_{p1}, M_{p2}) and (M_{n1}, M_{n2}). Since the phase shifter core provides 150° of phase tuning, the relative size of (M_{p1}, M_{p2}) and (M_{n1}, M_{n2}) are set such that the balun provides 150° of phase shift by inverting the logic state of SW_s. This allows for the output signal phase to be continuously tuned over a range of 300°.

The phase shifter core is shown in Fig. 2.8(b). The switched cascode transistors M_{S1R} and M_{S1L}, controlled by SW_1, and M_{S2R} and M_{S2L}, controlled by SW_2, are used to switch the varactors C_{var1} and C_{var2}. By using different combinations of SW_1 and SW_2 states (where at least one signal is at logic high), in conjunction with varying V_{ctrl} from 0 V to 1.5 V, the output differential phase can be continuously varied within a range of 150°. The phase tuning range is then increased up to 300° by inverting the logic state of SW_s. It should be noted that the phase tuning range of the phase shifter core could be increased to 180° through adding one more switched varactor (allowing for 360° of phase tuning by inverting the polarity of the differential signals). However, this approach would increase the output signal amplitude variation mainly due to the difference in varactors' parasitics (which changes C_P) in different switch states.

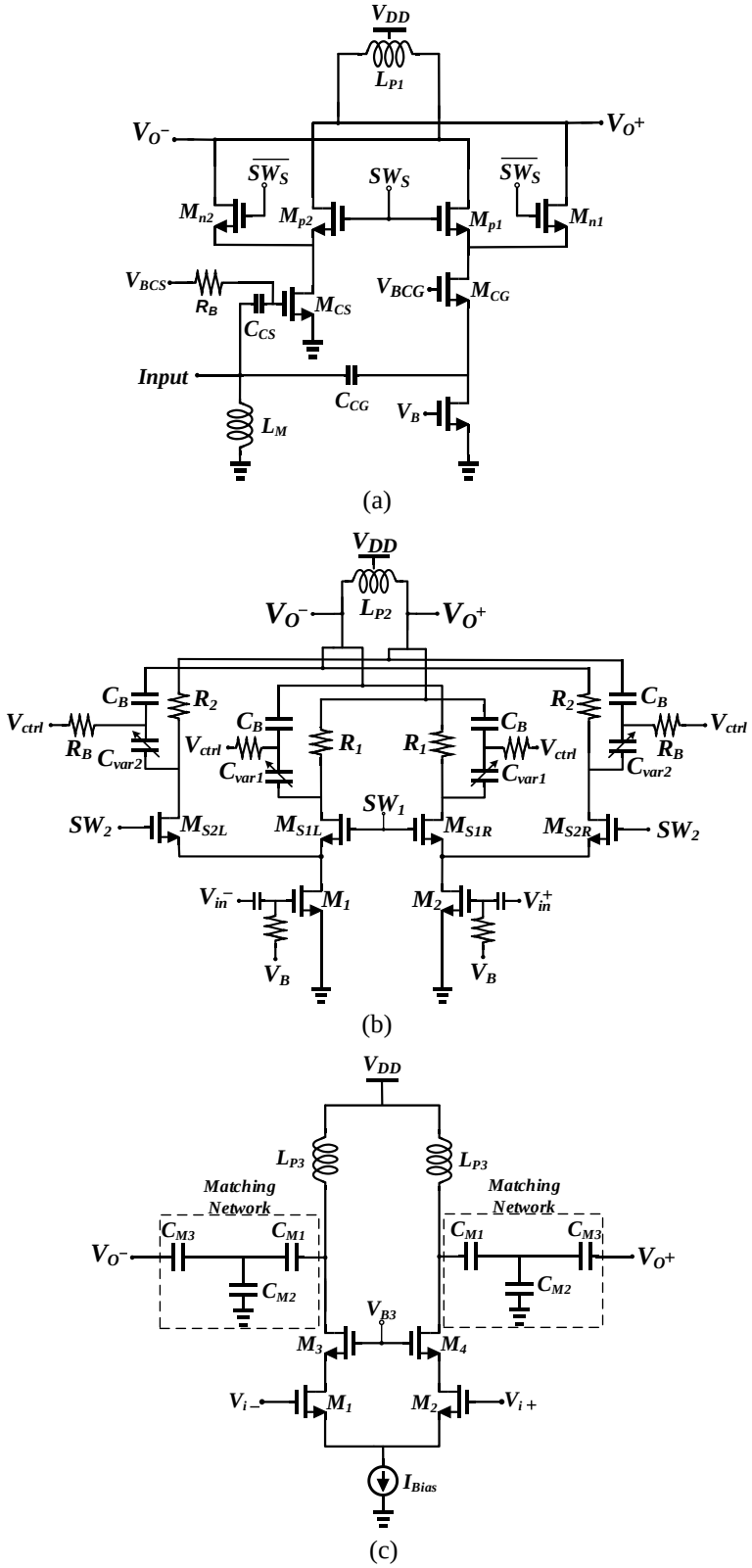


Fig. 2.8. Circuit diagrams for (a) active input balun (1st stage), (b) phase shifter core (2nd stage), and (c) output buffer (3rd stage).

The output buffer, shown in Fig. 2.8(c), is a differential circuit that isolates the phase shifter

core from the output load while matching the phase shifter's outputs to 50 Ω for measurement purposes. The utilized matching network includes several capacitors and excludes inductors to save the chip area.

2.4 Simulation and Measurement Results

Fig. 2.9 shows the die photo of the fabricated 130-nm CMOS phase shifter with a total die size of 1.170 × 1.214 mm^2. Measurements were performed by connecting the input and output pads to GSG and GSGSG 50 Ω probes (connected to a vector network analyzer), respectively.

Fig. 2.10 shows the simulated and measured frequency response of the phase shifter, in 16 different states for switches and control voltage, providing 16 uniformly distributed phase values within the entire phase tuning range at 23 GHz. The measured phase tuning range is 295° at 23 GHz which is close to its simulated value of 300° as shown in Fig. 2.10(a). The measurement results show that the phase shifter provides more than 290° of continuous phase tuning within 21−24 GHz. The simulated and measured results for the phase shifter gain versus frequency (obtained in the same cases as Fig. 2.10(a)) are shown in Fig. 2.10(b). The measured gain varies less than ±4.5 dB over the entire phase tuning range within 21−24 GHz. The simulated and

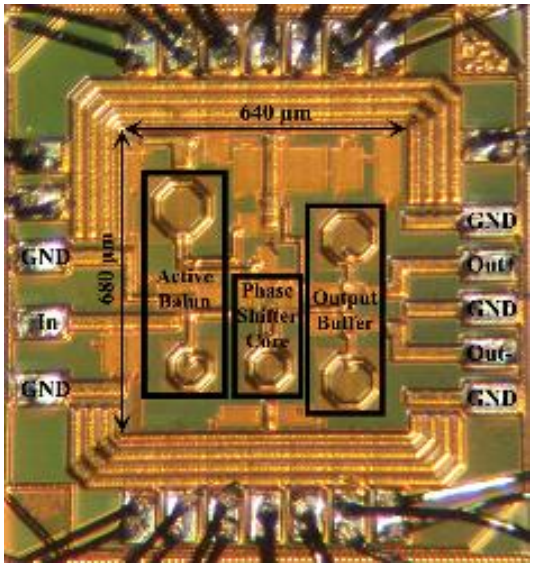
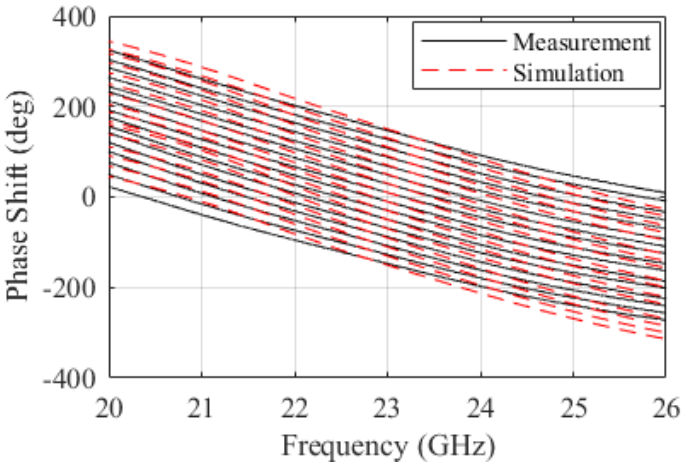
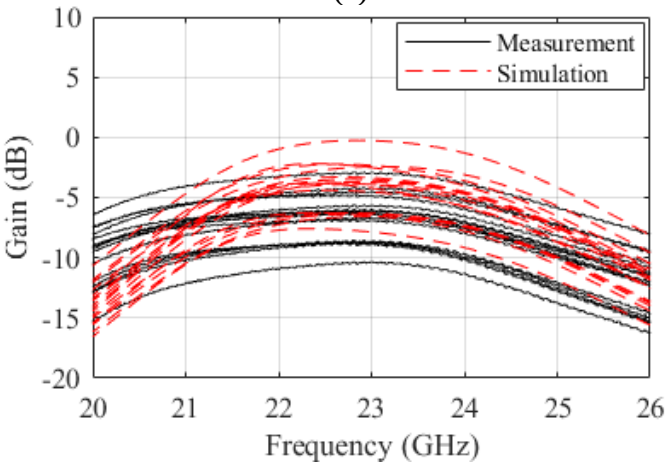


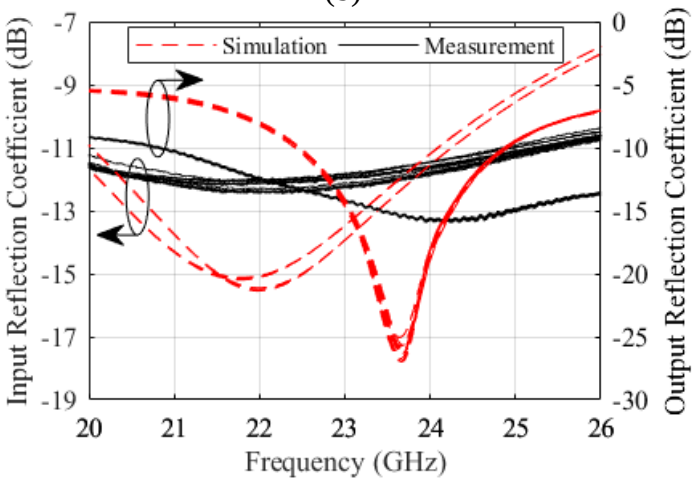
Fig. 2.9. Die photo of the fabricated phase shifter (die size = 1.170 mm × 1.214 mm).



(a)



(b)



(c)

Fig. 2.10. Simulated and measured (a) differential phase, (b) differential gain, and (c) input and output reflection coefficients versus frequency, for 16 uniformly distributed phase states within the entire phase tuning range at 23 GHz.

measured input and output reflection coefficients are shown in Fig. 2.10(c). The measured input and output reflection coefficients are less than -10 dB within the range 21−24 GHz. The difference

between the simulation and measurement results in Fig. 2.10 is mainly due to the limited accuracy of the electromagnetic modeling. The measured differential gain, shown in Fig. 2.10(b), is less than its simulated value, while the bandwidth in measurement results is larger than the simulation results. According to Fig. 2.10(a), the measurement results also show a smaller group delay compared to the simulation results. These differences between the simulation and measurement results is mainly due to the deviation of the resonant frequency of some stages form their simulated values. The deviation in resonance frequency of the 2nd stage (phase shifter core) could significantly change the phase tuning range. However, the measured phase tuning range is close to its simulated value. Therefore, apparently, the shift in resonance frequency has occurred for the 1st or 3rd stage (s). These differences between the simulation and measurement results can be minimized through a more accurate electromagnetic modeling of the circuit.

The RMS phase and gain errors for the 16 measured insertion phase and gain, shown in Fig. 2.11, are calculated based on the formulas provided in [34] and given in Eq. 2.16 and 2.17

$$\text{RMS Phase Error (deg)} = \sqrt{\frac{1}{N-1} \times \sum_{k=2}^{N} |\Delta\varphi_k|^2} \tag{2.16}$$

$$\text{RMS Gain Error (dB)} = \sqrt{\frac{1}{N} \times \sum_{k=1}^{N} |\Delta A_k|^2}\,, \tag{2.17}$$

where, N is 16, $\Delta\varphi_k$ represents the error between the *k*th output phase and the ideal phase value corresponding to the *k*th phase state among the 16 uniformly distributed phase values within the entire phase tuning range, and $\Delta A_k = A_k(\text{dB}) - A_{\text{average}}$. A_k is the insertion gain (in dB scale) corresponding to the *k*th output phase, and A_{average} (in dB-scale) is the average of the insertion gains

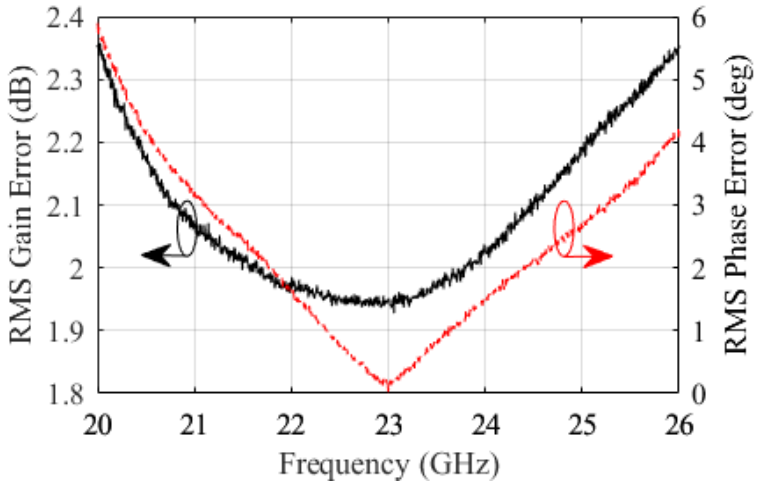


Fig. 2.11. Measured RMS phase and gain errors versus frequency calculated for 16 uniformly distributed phase states within the entire phase tuning range at 23 GHz.

in dB-scale. The measured RMS phase and gain errors are shown in Fig. 2.11. The RMS phase error is less than 3.2° and the RMS gain error is less than 2.1 dB within 21−24 GHz.

The measured differential gain and phase of the circuit at 23 GHz as a function of the control voltage for different switching states (SW_s, SW_2, SW_1) are shown in Fig. 2.12. The gain variation over the phase tuning range is less than 0.6 dB for (SW_s, SW_2, SW_1) = (1, 0, 1) and less than 1.4 dB for (SW_s, SW_2, SW_1) = (0, 0, 1), where the circuit is optimized for minimum output signal amplitude variation. These switching states correspond to approximately 66° of phase tuning. The optimum design condition for minimum gain variation over the phase tuning range could not be satisfied for other switching states of (SW_2, SW_1). This is mainly due to the difference in varactors' parasitics in different states that changes C_P and adding one path from the input to the output for (SW_2, SW_1) = (1, 1). The total gain variation range for different combinations of (SW_s, SW_2, SW_1) is less than 8.3 dB over the entire 295° of phase tuning at 23 GHz while the total gain variation in different combinations of (SW_2, SW_1), which corresponds to 147.5° of phase tuning at 23 GHz, is less than 5.8 dB. As shown in Fig. 2.12, to obtain 90° of phase tuning, one can set SW_s and SW_1 to 1 and vary V_{ctrl} from 0 V to 1.5 V when SW_2 is set to 0 and from 1.07 V to 1.35 V when SW_2

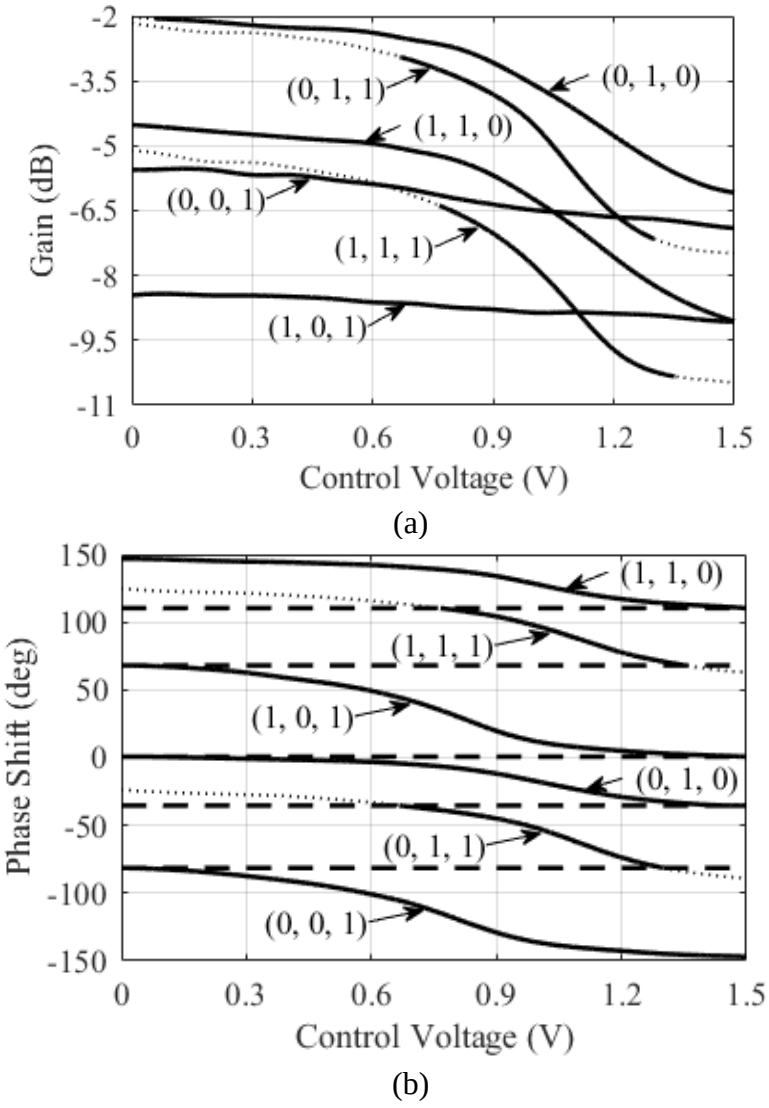
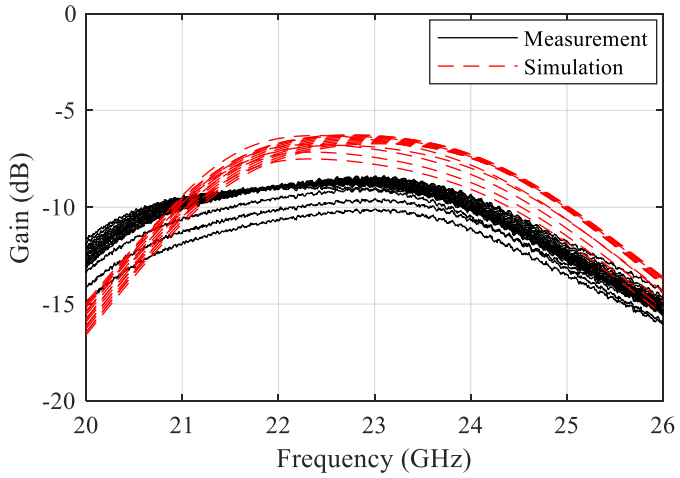
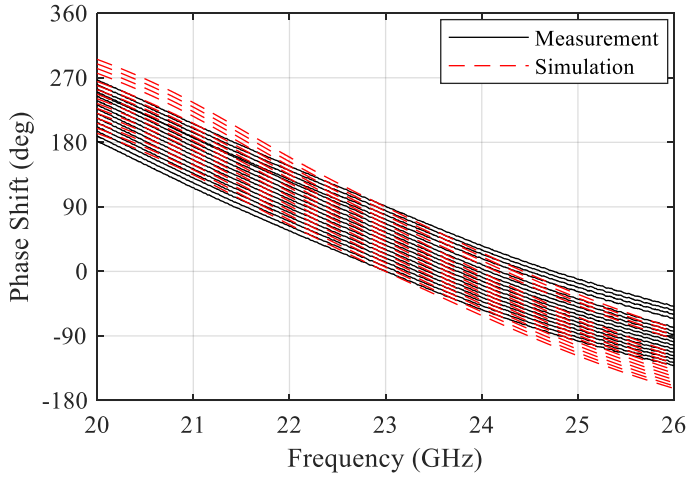


Fig. 2.12. Measured (a) differential gain and (b) differential phase at 23 GHz versus the control voltage for different switching states (SW_s, SW_2, SW_1).

is set to 1. Fig. 2.13 shows the simulated and measured differential phase and gain of the integrated phase shifter versus frequency for 90° of phase tuning range obtained through tuning V_{ctrl} and switching SW_2. The gain variation of the fabricated circuit over 90° of phase tuning range at 23 GHz is less than 1.5 dB and 1.8 dB in the simulation and measurement results, respectively. The circuit could provide a better performance if it was designed for only 90° of phase tuning using a single pair of identical varactors, as described in Section 2.2.3.



(a)



(b)

Fig. 2.13. Measured (a) differential gain and (b) differential phase versus frequency for 90° of phase tuning range which is obtained through tuning V_{ctrl} and switching SW_2.

The phase shifter's performance is summarized and compared to several RF vector modulator phase shifters in Table 2.2. The integrated vector modulator phase shifter presented in this work provides more than 290° of continuous phase tuning within the range 21−24 GHz. The IC consumes 18.5 mW of dc power, and its size excluding the pads is 0.64 mm×0.68 mm. The size of the phase shifter core is only 0.15 mm×0.3 mm and its dc power consumption is 7.8 mW. The phase shifter core employing multiple switched varactors consumes small power and occupies a

small chip area. However, the circuit exhibits a relatively large amplitude variation over the phase tuning range. The implementation could be better in terms of the output amplitude variation if a differential quadrature generation network was implemented along with the phase shifter core designed for 90° of phase tuning.

2.5 Conclusion

A new circuit topology for a single-stage vector modulator phase shifter has been presented. In this circuit, orthogonal vectors I and Q are generated, and their phases in conjunction with their amplitudes are simultaneously varied (while the relative phase between I and Q is preserved), by adjusting the value of a single pair of identical variable capacitors, to control the vector sum phase. Equal phase variation (rotation) of I and Q vectors contributes to varying the vector sum phase while maintaining the vector-sum magnitude. This results in reducing the phase shifter's gain/loss variation over a specific phase tuning range, or from another point of view, increasing the phase tuning range for a specific gain/loss variation. This chapter has presented a detailed analysis of the single-stage vector modulator phase shifter operating based on the summation of rotating orthogonal vectors. Moreover, a design methodology for maximizing the phase tuning range while maintaining the output signal amplitude over the phase variation range has been presented. The performance of a single-stage CMOS vector modulator phase shifter designed for maximum phase tuning range with a nearly constant output signal amplitude at K-band has been shown. The CMOS phase shifter, controlled by a single analog input, provides 90° of continuous phase tuning with a nearly constant output amplitude. Furthermore, an integrated phase shifter with a single-ended input and differential outputs whose core includes the presented fully-differential vector modulator circuit has been designed and fabricated at K-band in 130-nm CMOS process. The chip provides

Table 2.2. Comparison table for vector sum phase shifters

Reference	This Work	[33]	[46]	[47]	[48]	[49]
Process	130-nm CMOS	180-nm CMOS	65-nm CMOS	250-nm SiGe BiCMOS	90-nm CMOS	180-nm SiGe BiCMOS
Frequency (GHz)	21–24	15–20	2–20	8–12	57–64	15–35
Phase Tuning Range	> 290°	360°	360°	360°	360°	360°
Phase Resolution	Continuous	Continuous	10-bit	6-bit	Continuous	4-bit
Gain (dB)	-7.4±4.5	-5±5	-3.5±4.5	-4.5±2▪	-8.5±4.5•	-4.2±9.2▪
Power (mW)	18.5	> 112	92♦	110	34	25.2♠
Area (mm^2)	0.435* / 0.045**	0.722	2.16	1.646*	0.66	0.192**

*Excluding the pads, **Phase shifter core ♦ Excluding the buffer ▪Average gain •Estimated from the measurement results for one output ♠ Excluding the active balun

more than 290° of continuous phase tuning over the band 21−24 GHz with an average insertion loss of 6.7 dB at 23 GHz. It consumes 18.5 mW of dc power and occupies 0.64×0.68 mm^2 of area (excluding the pads). The dc power consumption of the phase shifter core is only 7.8 mW, and its corresponding area is 0.15×0.3 mm^2. Due to the compact size, low power consumption, and continuous phase tuning of this phase shifter, it is a potential candidate for integrated phased arrays.

Chapter 3: A Frequency-Tunable 360° Analog CMOS Phase Shifter with an Adjustable Output Amplitude

3.1 Introduction

Phase shifters' characteristics such as phase-shift precision and tuning range highly impact the arrays' beam forming and steering performance. Phase shifters and their associated control circuitry also highly impact the complexity and size of phased arrays. Due to the capability of the vector sum phase shifters to provide 360° of phase tuning while occupying a small area, multiple integrated phased arrays have utilized vector sum phase shifters to adjust the signal phase across the array elements [37] – [41]. Principle of operation of vector sum phase shifters is described in Chapter 2. In this chapter, a new circuit topology for a vector sum phase shifter is presented. In this circuit, all the tasks of vector generation, gain control, and vector summation are performed in a single block (phase shifter core) to save power and area. The phase shifter core provides 360° of continuous phase tuning with an adjustable output amplitude while consuming only 0.063 mm^2 of chip area. The phase shifter generates a signal with a tunable phase and magnitude in a phased array, thereby providing a better control over the beamwidth and sidelobe levels.

Most vector sum phase shifters perform the vector summation in the current domain [34], [37], [46], [50], [51]. The amplitudes of the orthogonal current signals are adjusted by controlling the gains of the I and Q transconductance stages. In the phase shifters reported in [34], [37], [50], this is achieved by tuning the bias currents of the I and Q transconductance stages. To generate a vector sum phase that is close to the phase of I (or Q) signal, a very large I and Q amplitude ratio is

required, necessitating very different bias currents for the I and Q transconductance stages [37]. This results in significantly different gain compression levels for I and Q paths, which cause an early phase distortion below the phase shifter's 1-dB gain compression point.

In the proposed vector sum phase shifter (where vector summation is performed in current domain), the gains of the I and Q transconductance stages are adjusted while the bias currents for the I and Q transconductance stages are kept equal and constant over the entire phase tuning range. The block diagram of the phase shifter is shown in Fig. 3.1. An active single-ended to differential signal converter (S2D) is used to convert the single-ended input signal to differential signals fed into a fully differential phase shifter core. In the phase shifter core, quadrature current signals (i_I^+, i_Q^+, i_I^-, and i_Q^-) are generated using a vector generation network. Several current steering variable gain amplifier (VGA)s are used to steer the quadrature currents in order to adjust the amplitudes of the currents added at the output of the phase shifter core while keeping the bias current of the I and Q transconductance stages constant. The four weighted current signals are then added to generate a signal with a tunable phase and magnitude. Furthermore, to save power and circuit area,

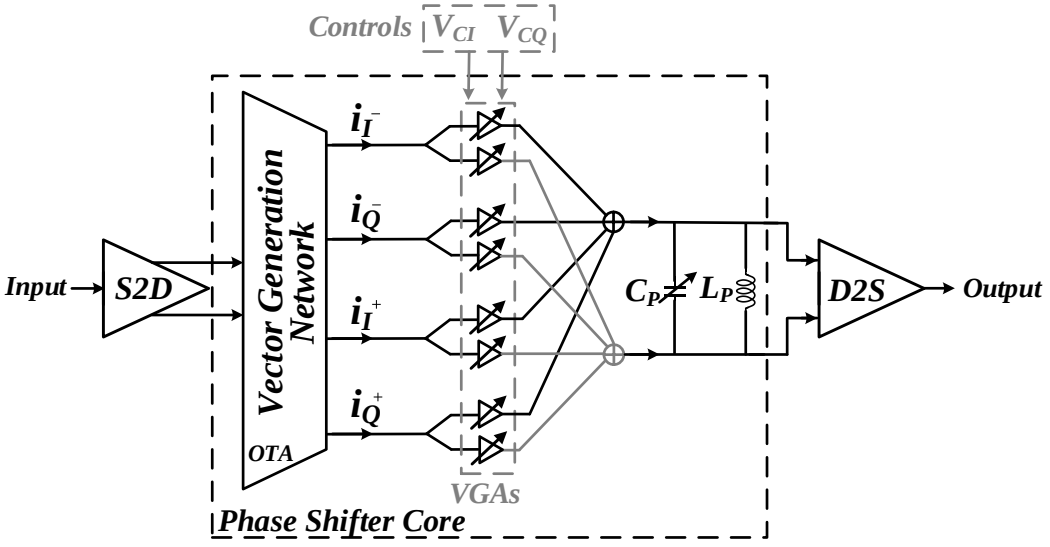


Fig. 3.1. Block diagram of the phase shifter designed within this work.

the variable gain amplifiers and the vector generation network are merged in a cascode configuration that performs all three tasks of vector generation, gain control, and vector summation. The last stage employs an active differential to single-ended signal converter (D2S) to convert the phase shifter core's differential output signals to a single-ended signal.

The phase shifter core can be utilized by itself in an integrated phased array with differential signaling. However, in this work, it is connected to an active single-ended to differential signal converter at the input and an active differential to single-ended signal converter at the output to allow for single ended measurements. Furthermore, the single-ended to differential signal converter and differential to single-ended signal converter stages are designed to satisfy the input and output matching to allow for phase shifter operation as a stand-alone IC. It should be noted that the employed active single-ended to differential signal converter and differential to single-ended signal converter stages occupy less area as compared to their passive counterparts.

In this work, an R-C poly phase filter (PPF) is utilized as the vector generation network due to its compact size as compared to transformer-based poly-phase networks [46], [51] and LC all pass filters [52]. A current mode R-C PPF is chosen over a voltage mode PPF since a current mode PPF has a higher input impedance and presents a larger load to its preceding stage, thereby reducing the overall system insertion loss [53]. Furthermore, in this work, unlike the phase shifters connecting the vector generation network to variable gain amplifiers through a buffer stage [46], [49], [51], PPF is directly connected to the current steering variable gain amplifiers in a cascode configuration. The impact of the variable gain amplifiers' input impedance variation (over thier gain tuning range) on the PPF is accounted for in the circuit design. The phase shifter provides 360° of continuous phase tuning with an adjustable output amplitude by tuning two control

voltages. The phase shifter exhibits a negligible phase distortion with input power variation up to 1-dB gain compression point.

This chapter is organized as follows. The phase shifter analysis and design are discussed in Section 3.2. The simulation and measurement results are presented in Section 3.3 followed by the conclusion provided in Section 3.4.

3.2 Phase Shifter Analysis and Design

The circuit diagrams for single-ended to differential signal converter, phase shifter core (2nd stage), and differential to signle-ended signal converter, which are all ac coupled, are shown in Fig. 3.2.

The utilized single-ended to differential signal converter, shown in Fig. 3.2(a), is based on a common-gate stage in parallel with a common-source stage [45]. The single-ended to differential signal convertedr is designed to satisfy the input matching requirement while generating differential output signals v_{o}^{+} and v_{o}^{-} that are fed into the phase shifter core [Fig. 3.2(b)]. The inductor L_{P1} and the variable capacitor C_{P1} are used to tune the center frequency of operation (f_{c}) within 26–28 GHz.

In the phase shifter core with differential inputs and outputs, shown in Fig. 3.2(b), a current mode R-C PPF along with transistors M_{p1}–M_{p4} are utilized to generate quadrature currents (i_{Q}^{+}, i_{I}^{+}, i_{Q}^{-}, and i_{I}^{-}). The transistors M_{p1}–M_{p4} have the same size and bias current. The magnitudes of the quadrature currents combined at the output are adjusted using current steering variable gain amplifier (VGA)s formed by the same-size transistors M_1–M_8. The variable gain amplifiers are controlled by voltages V_{CQ} and V_{CI} applied to the gates of the transistors (M_2, M_5) and (M_4, M_7), respectively. It should be noted that transistors $M_1$and M_6, M_2 and M_5, M_3 and M_8 as well as M_4

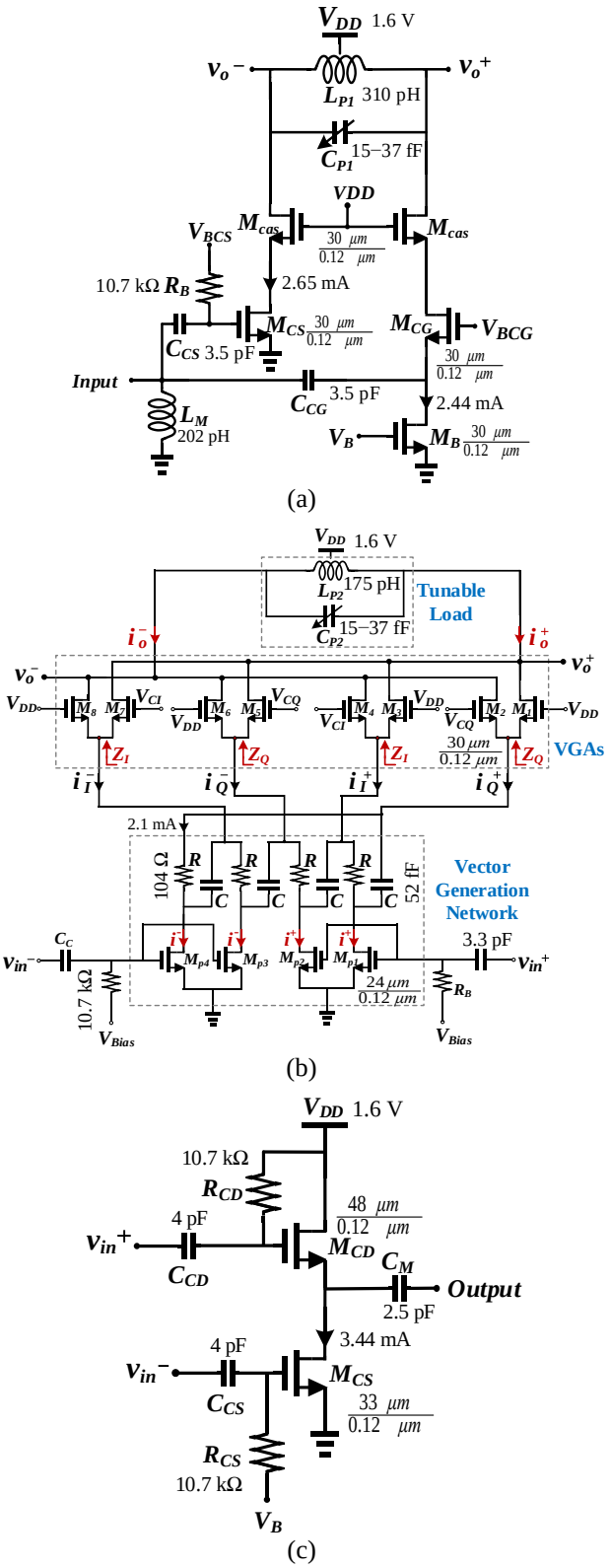


Fig. 3.2. Circuit diagrams for (a) single-ended to differential signal converter, (b) phase shifter core, and (c) differential to single-ended signal converter.

and M_7 have identical small signal parameters since thay have the same size and equal bias currents

for all values of V_{CQ} and V_{CI}.

The currents i_{Q}^{+}, i_{I}^{+}, i_{Q}^{-}, and i_{I}^{-} are given by:

$$i_{\mathrm{Q}}^{\pm} = i^{\pm}\frac{RCj\omega - 1}{1 + RCj\omega(1 + 2\frac{Z_{\mathrm{Q}}}{R})} \tag{3.1}$$

$$i_{\mathrm{I}}^{\pm} = i^{\pm}\frac{RCj\omega + 1}{1 + RCj\omega(1 + 2\frac{Z_{\mathrm{I}}}{R})}. \tag{3.2}$$

where i^{+} and i^{-} are the small signal drain currents of the transistors (M_{p1}, M_{p2}) and (M_{p3}, M_{p4}), respectively, and Z_{Q} and Z_{I} are the impednaces looking into the source nodes of the current steering variable gain amplifier (VGA)s as shown in Fig. 3.2(b). According to Eq. (3.1) and Eq. (3.2), i_{Q}^{+} and i_{Q}^{-} as well as i_{I}^{+} and i_{I}^{-} are equal in magnitude and 180° out of phase.

The currents i_{Q}^{+}, i_{I}^{+}, i_{Q}^{-}, and i_{I}^{-} have quadrature phases and equal magnitudes if $RC\omega$ = 1 and Z_{Q} = Z_{I}. The values of R and C are selected such that $RC\omega$ = 1 at the center frequency of operation (ω_{c}). However, Z_{Q} and Z_{I} are not necessarily identical since they are functions of V_{CQ} and V_{CI}. The dependency of Z_{Q} and Z_{I} on the control voltages, V_{CQ} and V_{CI}, can be calculated. Assuming a negligible output transconductance for the MOS transistors ($g_{\mathrm{ds}} \ll g_{\mathrm{m}}$), Z_{Q} and Z_{I} are given by:

$$Z_{\mathrm{Q}} = \frac{1}{Y_{\mathrm{Q}}} = \frac{1}{G_{\mathrm{Q}} + jB_{\mathrm{Q}}} = \frac{1}{g_{\mathrm{m1}} + g_{\mathrm{m2}} + j\omega C_{\mathrm{pQ}}} \tag{3.3a}$$

$$Z_{\mathrm{I}} = \frac{1}{Y_{\mathrm{I}}} = \frac{1}{G_{\mathrm{I}} + jB_{\mathrm{I}}} = \frac{1}{g_{\mathrm{m3}} + g_{\mathrm{m4}} + j\omega C_{\mathrm{pI}}} \tag{3.3b}$$

where C_{pQ} and C_{pI} are the parasitic capacitances looking into the source nodes of the current steering variable gain amplifiers in Q and I paths, respectively, and g_{mk} (k = 1, 2, 3, and 4) is the transconductance of the transistor M_{k}. Utilizing long channel I-V approximations for MOS transistors, the transconductance g_{mk} is given by $\sqrt{2I_{\mathrm{k}}\mu_{\mathrm{n}}C_{\mathrm{ox}}\,(W/L)}$ where μ_{n} is the electron

mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the transistor width and length, and I_{k} is the bias current of the transistor M_{k}. Neglecting the subthreshold conduction, the conductances G_{Q} (= g_{m1} + g_{m2}) and G_{I} (= g_{m3} + g_{m4}) in Eq. (3.3) are given by:

$$G_{\mathrm{Q,I}} = \sqrt{4KI_{\mathrm{B}} - \left(K\Delta V_{\mathrm{Q,I}}\right)^2} \qquad \left|\Delta V_{\mathrm{Q,I}}\right| \le \sqrt{2I_{\mathrm{B}}/K} \tag{3.4}$$

where $K = \mu_{\mathrm{n}} C_{\mathrm{ox}} \left(\frac{W}{L}\right)$, $\Delta V_{\mathrm{Q,I}} = V_{\mathrm{DD}} - V_{\mathrm{CQ,I}}$, and $I_{\mathrm{B}} = I_{\mathrm{k}} + I_{\mathrm{k+1}}$ (k = 1, 3, 5, and 7). Due to the dependency of G_{Q} and G_{I} on the control voltages, the variable gain amplifiers' input impedances (Z_{Q} and Z_{I}) are functions of V_{CQ} and V_{CI} (according to (3.3)). Therefore, the amplitudes and phases of the signals generated by the vector generation network are also functions of V_{CI} and V_{CQ}. To estimate the control voltages of V_{CI} and V_{CQ} required for a desired insertion phase and gain, the small signal output voltage v_{o} (= $v_{\mathrm{o}}^{+} - v_{\mathrm{o}}^{-}$) is calculated as a function of V_{CI} and V_{CQ}. The output voltage v_{o} is given by:

$$v_{\mathrm{o}} = -\frac{1}{2} Z_{\mathrm{out}} \left(i_{\mathrm{Q}}^{+} \underbrace{Z_{\mathrm{Q}}(g_{\mathrm{m1}} - g_{\mathrm{m5}})}_{A_{\mathrm{Q}}} + i_{\mathrm{I}}^{+} \underbrace{Z_{\mathrm{I}}(g_{\mathrm{m3}} - g_{\mathrm{m7}})}_{A_{\mathrm{I}}} \right) \tag{3.5}$$

where A_{Q} and A_{I} are the current gains of the variable gain amplifiers adjusting the magnitudes of the Q and I vectors, respectively. Z_{out} denotes the output impedance of the phase shifter core including the inductor L_{P2}, variable capacitor C_{P2} (used to tune the operation frequency), and the parasitic capacitances C_{gd} and C_{db} of M_1–M_8. Since g_{m5} = g_{m2}, and g_{m7} = g_{m4}, Eq. (3.5) can be rewritten as

$$v_{\mathrm{o}} = -\frac{1}{2} Z_{\mathrm{out}} \left(i_{\mathrm{Q}}^{+} \underbrace{Z_{\mathrm{Q}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})}_{A_{\mathrm{Q}}} + i_{\mathrm{I}}^{+} \underbrace{Z_{\mathrm{I}}(g_{\mathrm{m3}} - g_{\mathrm{m4}})}_{A_{\mathrm{I}}} \right) \tag{3.6}$$

where

$$g_{\mathrm{m1}} - g_{\mathrm{m2}} = K\Delta V_{\mathrm{Q}} \qquad \left|\Delta V_{\mathrm{Q}}\right| \le \sqrt{2I_{\mathrm{B}}/K} \tag{3.7a}$$

$$g_{m3} - g_{m4} = K\Delta V_I \qquad |\Delta V_I| \le \sqrt{2I_B/K}. \tag{3.7b}$$

By substituting Eq. (3.1), (3.2), and (3.3) in (3.6), the phase and magnitude of v_o (small signal output voltage of the phase shifter core) at ω_c are given by:

$$\measuredangle v_o = tan^{-1}\left(\frac{y}{x}\right) + \measuredangle i^+ + \measuredangle Z_{out}(j\omega_c), \tag{3.8a}$$

$$|v_o| = \frac{1}{2}|i^+ Z_{out}(j\omega_c)|\sqrt{x^2 + y^2} \tag{3.8b}$$

where

$$x = \frac{(g_{m4} - g_{m3})\left(G_I + {}^1\!/_R\right)}{\left(G_I + {}^1\!/_R\right)^2 + \left(\omega_c C_{pI} + {}^1\!/_R\right)^2} + \frac{(g_{m2} - g_{m1})\left(\omega_c C_{pQ} + {}^1\!/_R\right)}{\left(G_Q + {}^1\!/_R\right)^2 + \left(\omega_c C_{pQ} + {}^1\!/_R\right)^2} \tag{3.9a}$$

$$y = \frac{(g_{m3} - g_{m4})\left(\omega_c C_{pI} + {}^1\!/_R\right)}{\left(G_I + {}^1\!/_R\right)^2 + \left(\omega_c C_{pI} + {}^1\!/_R\right)^2} + \frac{(g_{m2} - g_{m1})\left(G_Q + {}^1\!/_R\right)}{\left(G_Q + {}^1\!/_R\right)^2 + \left(\omega_c C_{pQ} + {}^1\!/_R\right)^2}. \tag{3.9b}$$

By using Eq. (3.7) and substituting G_Q and G_I, from Eq. (3.4), into Eq. (3.9), the phase and magnitude of v_o at ω_c can be calculated as a function of V_{CI} and V_{CQ}. The values of V_{CI} and V_{CQ} for a desired output phase and magnitude can be obtained by solving Eq. (3.8a) and (3.8b).

The differential to single-ended signal converter, shown in Fig. 3.2(c), converts the differential signals at the output of the phase shifter core to a single-ended signal. The differential to single-ended signal converter is designed to match the output to 50 Ω for measurement purposes.

3.3 Simulation and Measurement Results

The phase shifter is fabricated in 130-nm CMOS process. The die photo of the fabricated phase shifter is shown in Fig. 3.3. The total die size including the pads is 1.187 mm × 0.72 mm. The performance of the chip is characterized using a probe station with GSG probes. Fig. 3.4 shows the polar plot of the simulated and measured forward transmission coefficient of the phase shifter

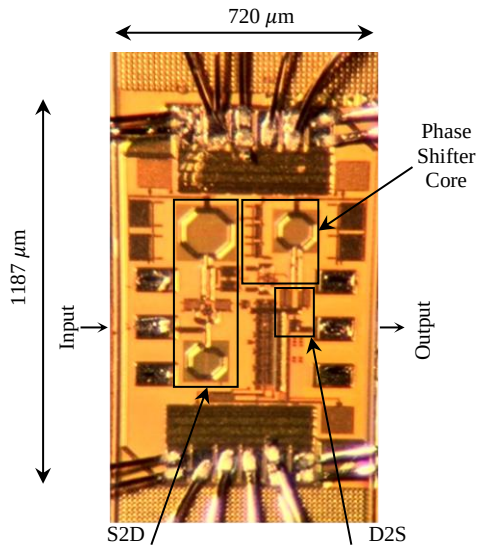
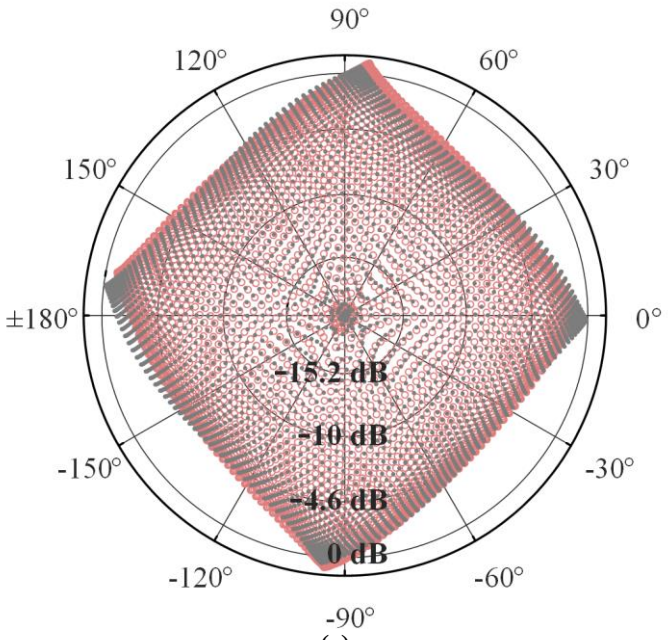


Fig. 3.3. Die photo of the fabricated phase shifter.

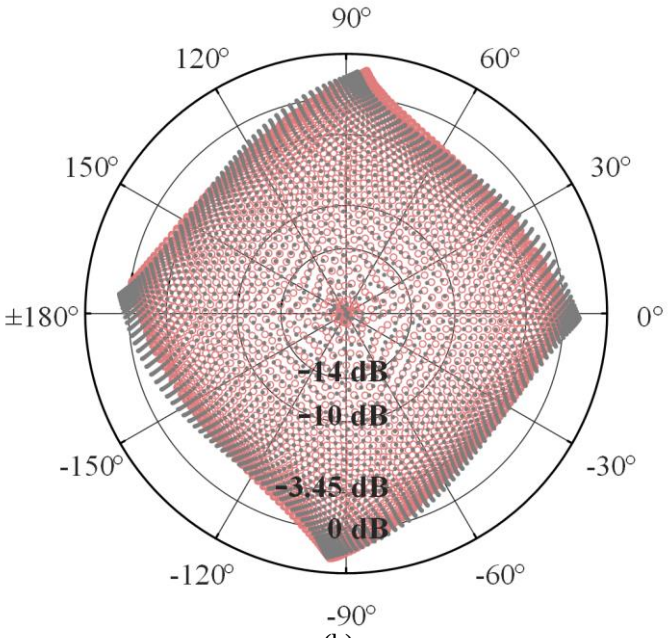
when the center frequency of operation (f_c) is set to 26 GHz and 28 GHz. The points in the figures correspond to the magnitude (in dB) and phase (in degrees) of the transmission coefficient while the two control voltages vary from 1.24 V to 1.96 V with a step size of 11.25 mV.

As shown in Fig. 3.4, the simulation and measurement results for the insertion phase and gain of the phase shifter are in good agreement. Considering the measured phases and magnitudes at 26 GHz (Fig. 3.4(a)), the described circuit can operate as a 6-bit 360° phase shifter with 10.6 dB of gain tuning range (from -15.2 dB to -4.6 dB) while exhibiting an RMS phase error of less than 1.6° and an RMS gain error of less than 0.5 dB at 26 GHz. When the phase shifter is tuned to operate at f_c=28 GHz, the gain can be varied from -14 dB to -3.45 dB while RMS phase and gain errors are limited to 1.54° and 0.5 dB, respectively.

The frequency response of the phase shifter when its center frequency is set to 26 GHz and 28 GHz is shown in Fig. 3.5. Insertion phase and gain of the phase shifter are simulated and measured for 64 uniformly distributed phase states from 0° to 360° with the maximum achievable gain at the center frequency of operation. The simulated and measured frequency response are shown for only 16 (out of the 64) cases in Fig. 3.5 (for a better graph visibility).



(a)



(b)

Fig. 3.4. Polar plot (magnitude in dB, phase in degree) of the phase shifter's transmission coefficient at (a) 26 GHz and (b) 28 GHz (circles: measurement, dots: simulation). Control voltages are varied from 1.24 V to 1.96 V with a step size of 11.25 mV.

The RMS phase and gain errors for the 64 measured cases are calculated using the formulas provided in [34]. As shown in Fig. 3.6, for the phase shifter operating at the center frequency of 26 GHz, the RMS phase and gain errors within the 3-dB bandwidth (24.55–27.4 GHz) are less than 2.6° and 0.31 dB, while the phase shifter operating at the center frequency of 28 GHz exhibits

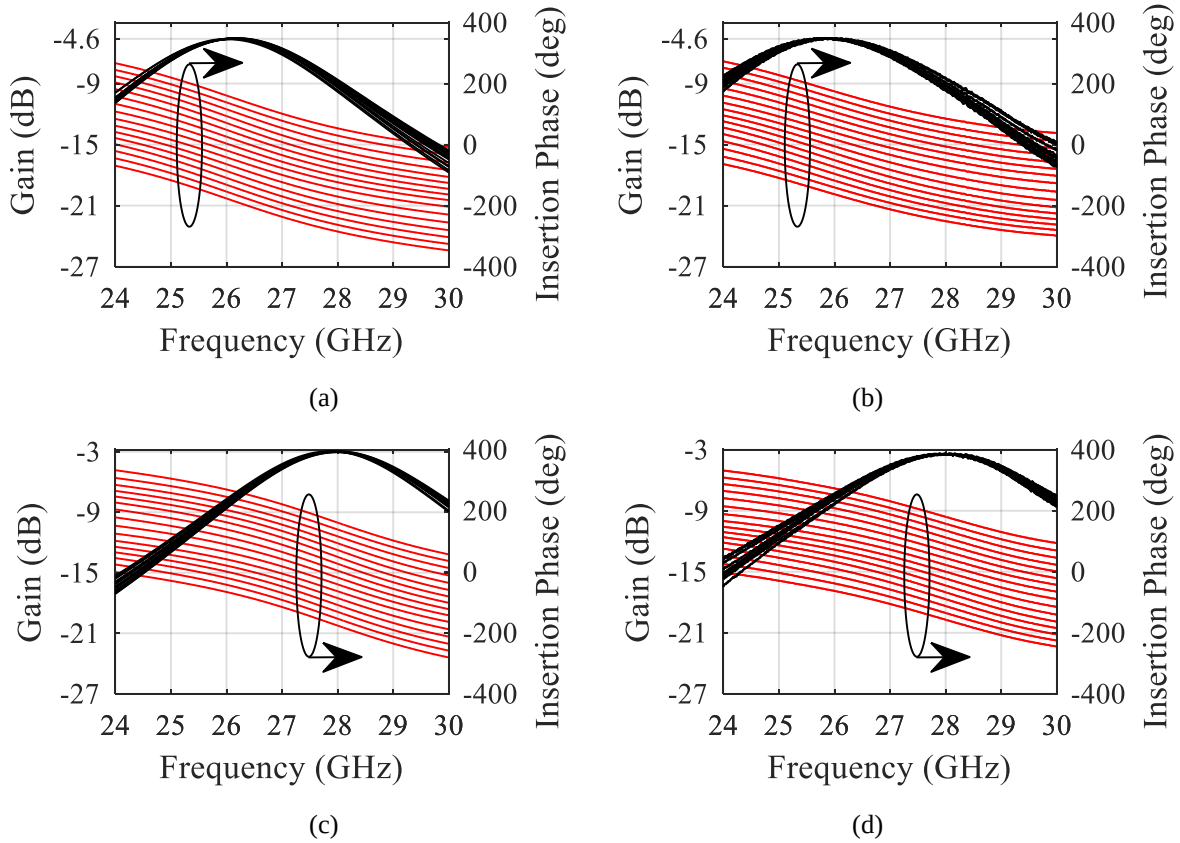


Fig. 3.5. Gain and phase response of the phase shifter. (a) Simulation and (b) measurement results for the phase shifter operating at the center frequency of 26 GHz. (c) Simulation and (d) measurement results for the phase shifter operating at the center frequency of 28 GHz.

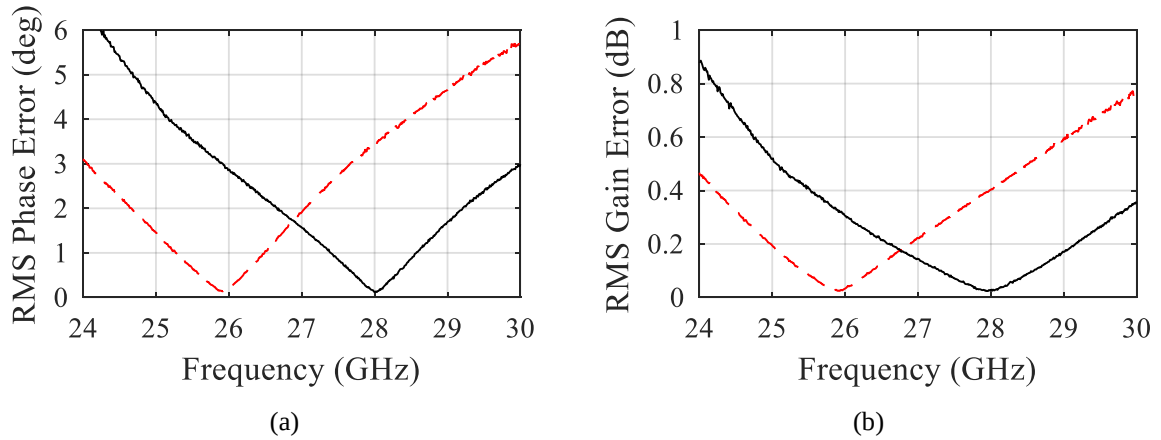
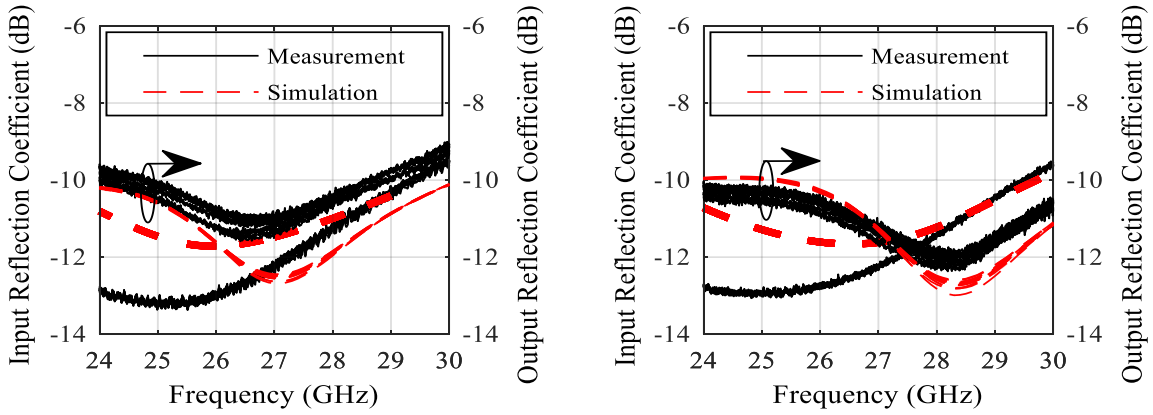


Fig. 3.6. Measured RMS (a) phase error and (b) gain error for the phase shifter operating at the center frequency of 26 GHz (dashed line) and 28 GHz (solid line).

an RMS phase error of less than 2.3° and RMS gain error of less than 0.25 dB within the 3-dB bandwidth (26.55–29.4 GHz). The RMS phase error is well below the resolution of a 6-bit phase shifter (5.625°) within the 3-dB bandwidth centered at 26 GHz and 28 GHz.



(a) (b)

Fig. 3.7. Simulated and measured input and output reflection coefficient of the phase shifter operating at the center frequency of (a) 26 GHz and (b) 28 GHz.

The simulated and measured input and output reflection coefficient for the phase shifter operating at the center frequency of 26 and 28 GHz are shown in Fig. 3.7. According to the simulation and measurement results, the input and output reflection coefficients are less than -10 dB over the operation band. It should be noted that the resonance frequency of the output matching network is related to the resonance frequency of the phase shifter core's output load. As a result, as shown in Fig. 3.7, resonance frequency of the output matching network is shifted by tuning the variable capacitor at the output of the phase shifter core. The input matching network is also designed to provide a reflection coefficient less than -10 dB over the operation band. The center frequency of the input matching network, in simulation results, is close to the center frequency of operation band. However, measurement results show that the center frequency of the input matching network is shifted by less than 1.5 GHz, which is due to the inaccuracy of the pad model or electromagnetic modeling of the inductors and transmission lines.

Fig. 3.8(a) and (b) show the measured input 1-dB compression points (IP1dB) versus frequency for 16 phase states at the center frequency of 26 and 28 GHz, respectively. The phase shifter's

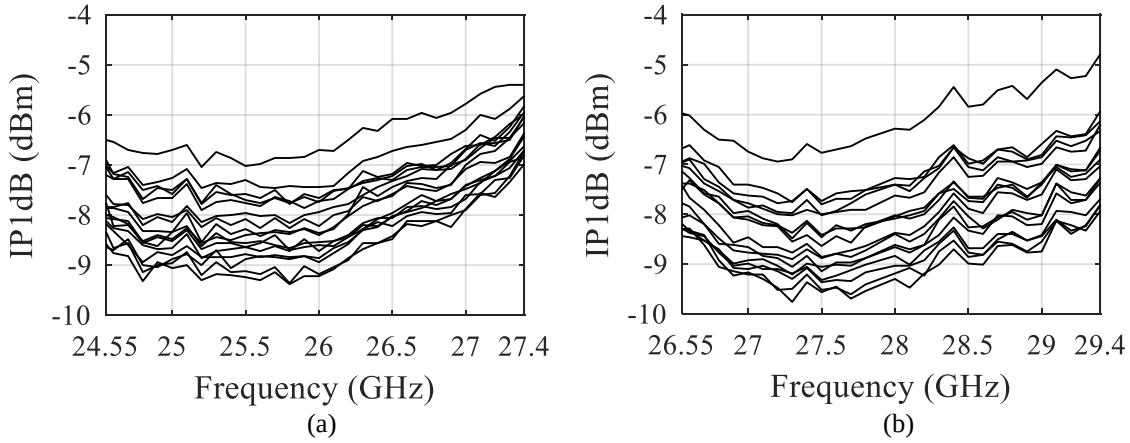


Fig. 3.8. Measured input 1-dB compression points (IP1dB) versus frequency for 16 phase states. The phase shifter operates at the center frequency of (a) 26 GHz and (b) 28 GHz.

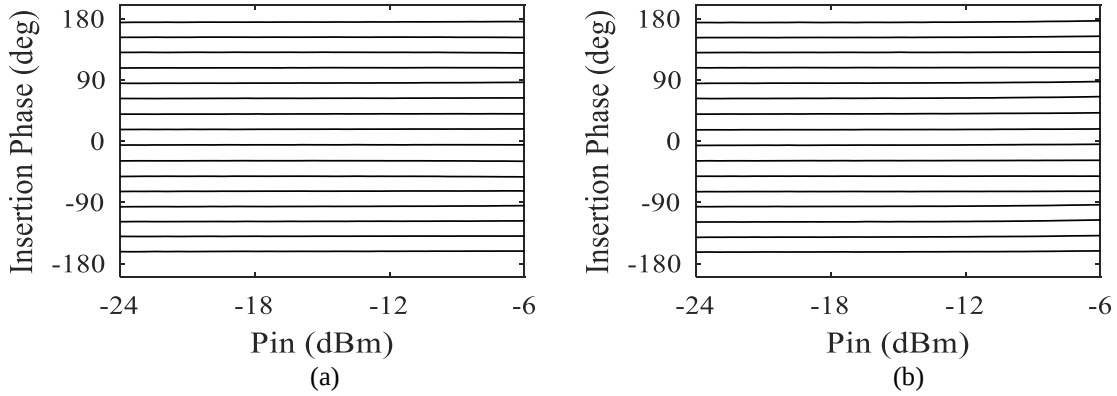


Fig. 3.9. Measured insertion phase versus input power (for 16 phase states) for the center frequency of (a) 26 GHz and (b) 28 GHz.

input 1-dB compression point for all phase states is larger than -9.8 dBm within the 3-dB bandwidth. The minimum measured IIP3 for the phase shifter at 26 and 28 GHz is 0 dBm.

Fig. 3.9(a) and (b) show the measured insertion phase versus input power for the phase shifter tuned at the center frequency of 26 and 28 GHz, respectively. Phase deviation for the input power levels up to the 1-dB compression point is less than 1.3° and 1.6° for the phase shifter operating at the center frequency of 26 and 28 GHz, respectively.

To show the sensitivity of the phase shifter to process, voltage, and temperature (PVT), the phase shifter is simulated for different values of V_{DD} in different process corners of tt (typical corner for NMOS and PMOS transistors), ff (fast corner for NMOS and PMOS transistors), and

ss[1] (slow corner for NMOS and PMOS transistors) and at different temperatures. Fig. 3.10 shows the frequency response of the phase shifter in several different conditions. As shown in Fig. 3.10, gain and insertion phase of the phase shifter are highly sensitive to the value of V_{DD}. The main reason is that operation of the variable gain amplifiers in the phase shifter core is a function of ΔV_I and ΔV_Q which are dependent on V_{DD} as well as V_{CI} and V_{CQ}. However, the errors in ΔV_I and ΔV_Q caused by the variation of V_{DD} can be corrected by tuning V_{CI} and V_{CQ} accordingly. To find the suitable control voltages that can compensate for the phase and gain errors in a specific case, one can plot the insertion phase and gain of the phase shifter as functions of V_{CI} and V_{CQ} and take the contour plots of constant gain (gain values that is maintained over the entire phase tuning range) into account.

[1] Fast, slow, and typical corners refer to the speed of operation for MOS transistors, which is mainly a function of transistors' threshold voltage and carrier mobilities.

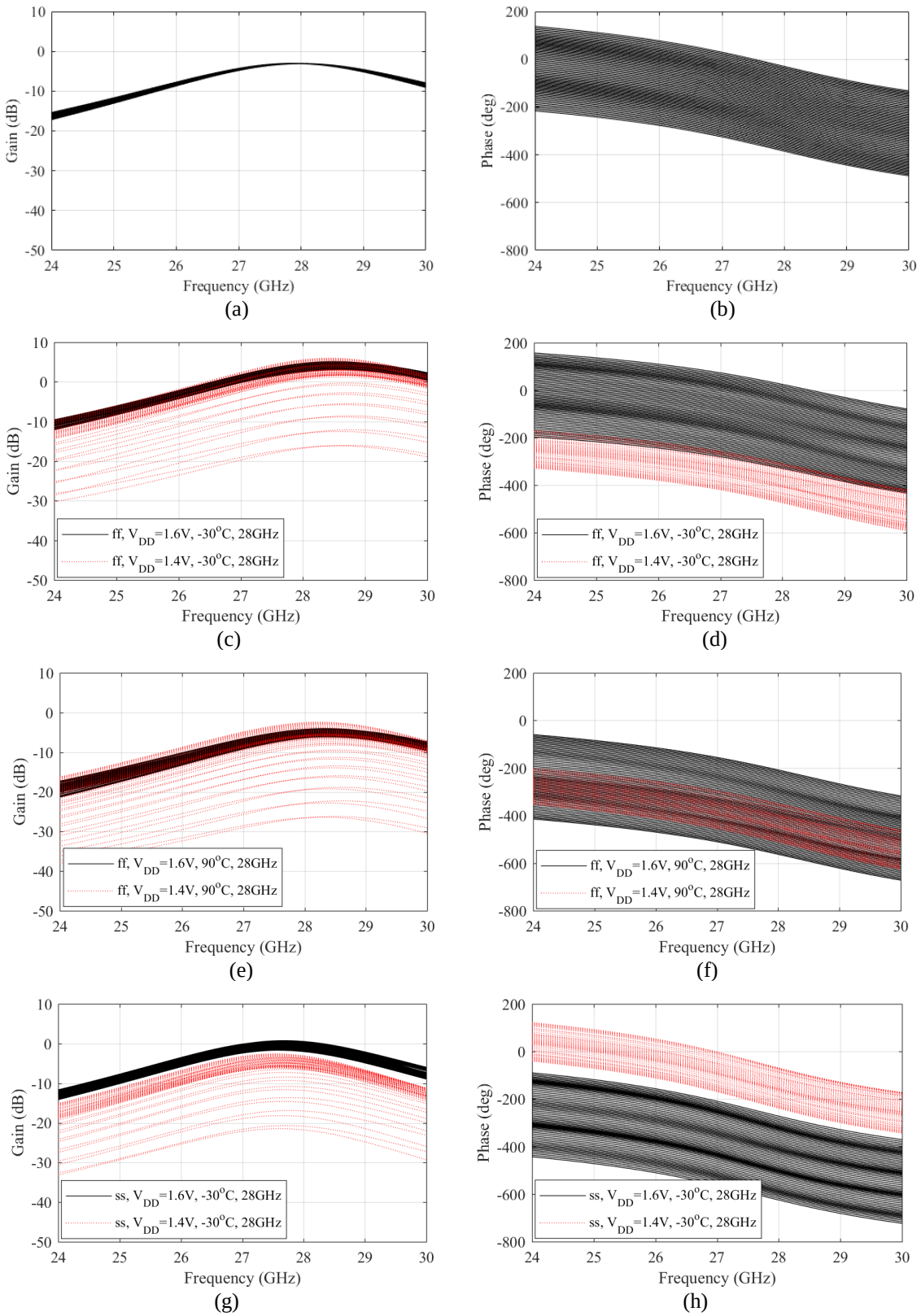


Fig. 3.10. (a) Gain and (b) phase versus frequency at nominal operating condition (tt, V_{DD}=1.6 V, 27 °C) for 64 selected control voltages. (c) Gain and (d) phase response of the phase shifter in the corner case of ff at -30 °C for V_{DD}=1.6 V and 1.4 V. (e) Gain and (f) phase response of the phase shifter in the corner case of ff at 90 °C for V_{DD}=1.6 V and 1.4 V. (g) Gain and (h) phase response of the phase shifter in the corner case of ss at -30 °C for V_{DD}=1.6 V and 1.4 V.

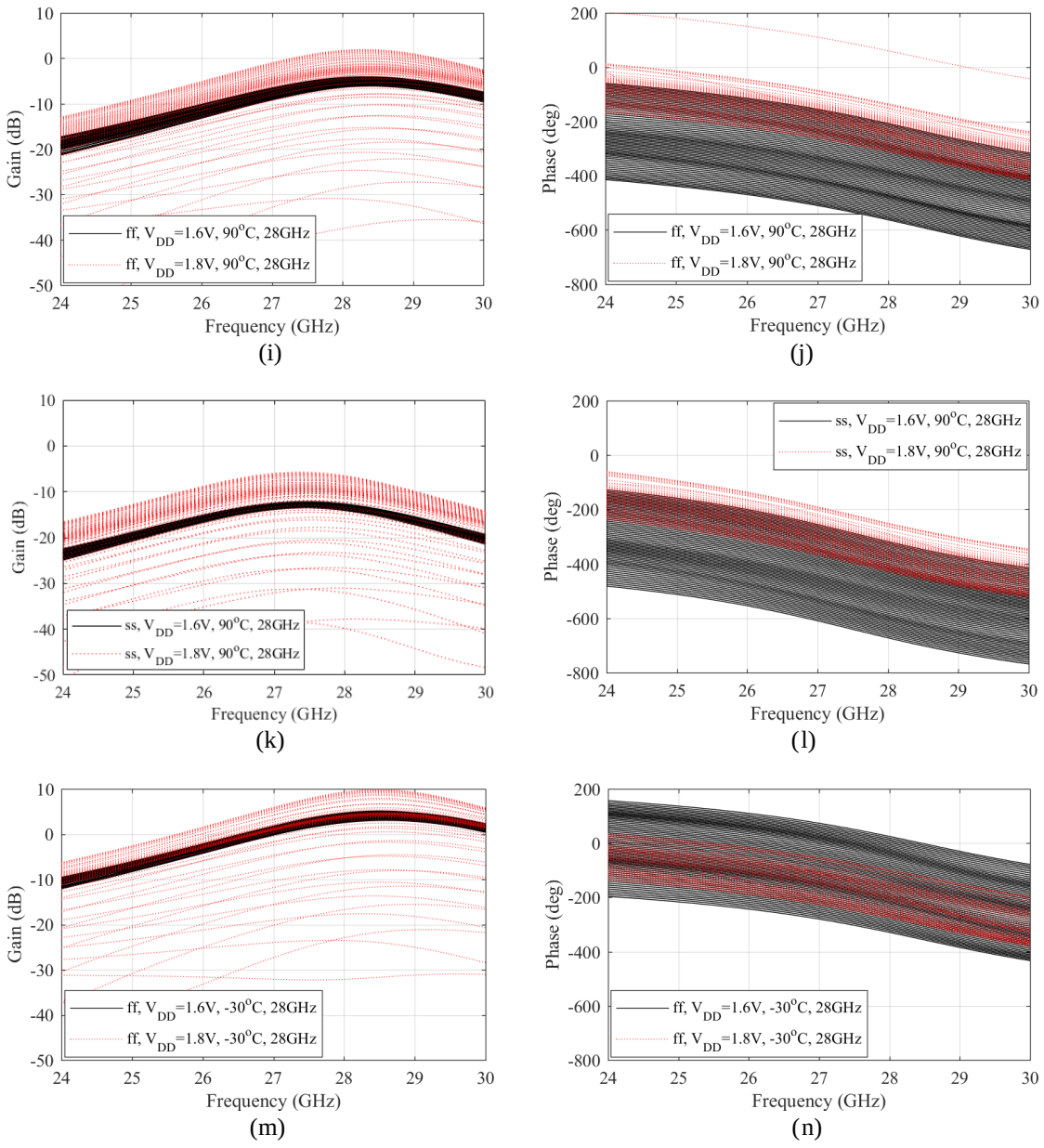
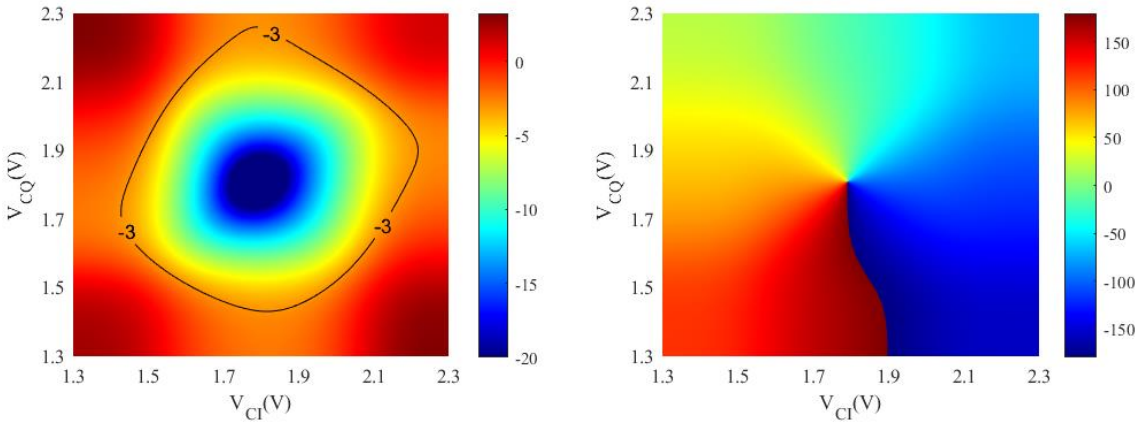


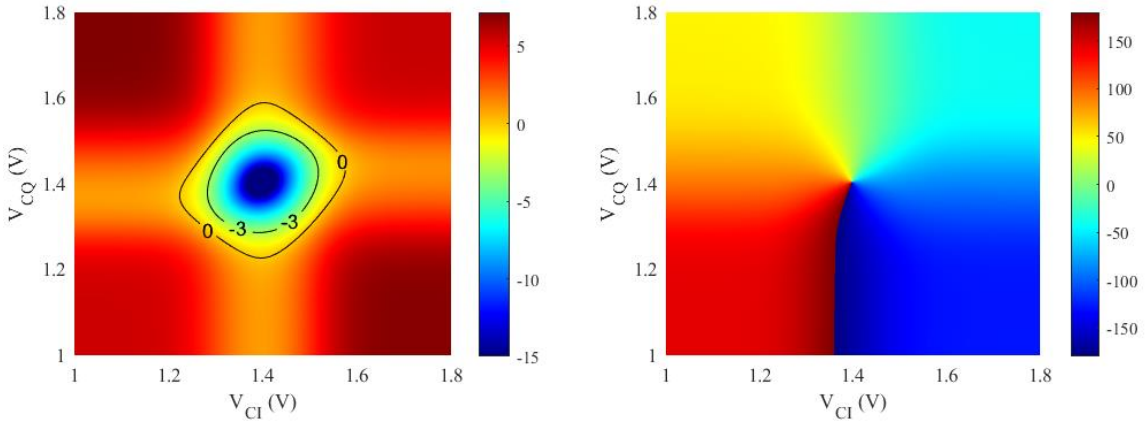
Fig. 3.10. (i) Gain and (j) phase response of the phase shifter in the corner case of ff at 90 °C for V_{DD}=1.6 V and 1.8 V. (k) Gain and (l) phase response of the phase shifter in the corner case of ss at 90 °C for V_{DD}=1.6 V and 1.8 V. (m) Gain and (n) phase response of the phase shifter in the corner case of ff at -30 °C for V_{DD}=1.6 V and 1.8 V.

Fig. 3.11 shows the insertion phase and gain of the phase shifter for different values of V_{CI} and V_{CQ} in the corner cases of (ff, V_{DD} = 1.8 V, 90 °C) and (ff, V_{DD} = 1.4 V, -30 ºC) at 28 GHz. As shown in Fig. 3.11, the maximum achievable constant gain in the corner (ff, V_{DD} = 1.8 V, 90 ºC)

is the same as the maximum constant gain in the nominal case (tt, V_{DD} = 1.6 V, 27 °C), while the maximum achievable constant gain in the corner (ff, V_{DD} = 1.4 V, -30 °C) is more than the maximum constant gain of the nominal case. To correct the phase and gain errors in the corner (ff, V_{DD} = 1.4 V, -30 °C), it is sufficient to tune the control voltages of V_{CI} and V_{CQ} and select the pairs of V_{CI} and V_{CQ} providing a constant gain equal to the maximum achievable constant gain in the nominal condition. As shown in Fig. 3.11, by adjusting V_{CI} and V_{CQ} in a specific manner, constant gain of -3 dB (equal to the maximum achievable constant gain for the nominal case in simulation results) can be obtained. In general, for the corner cases in which the maximum achievable constant gain is more than the gain obtained for the nominal case of (tt, V_{DD} =1.6 V, 27 °C), the phase shifter

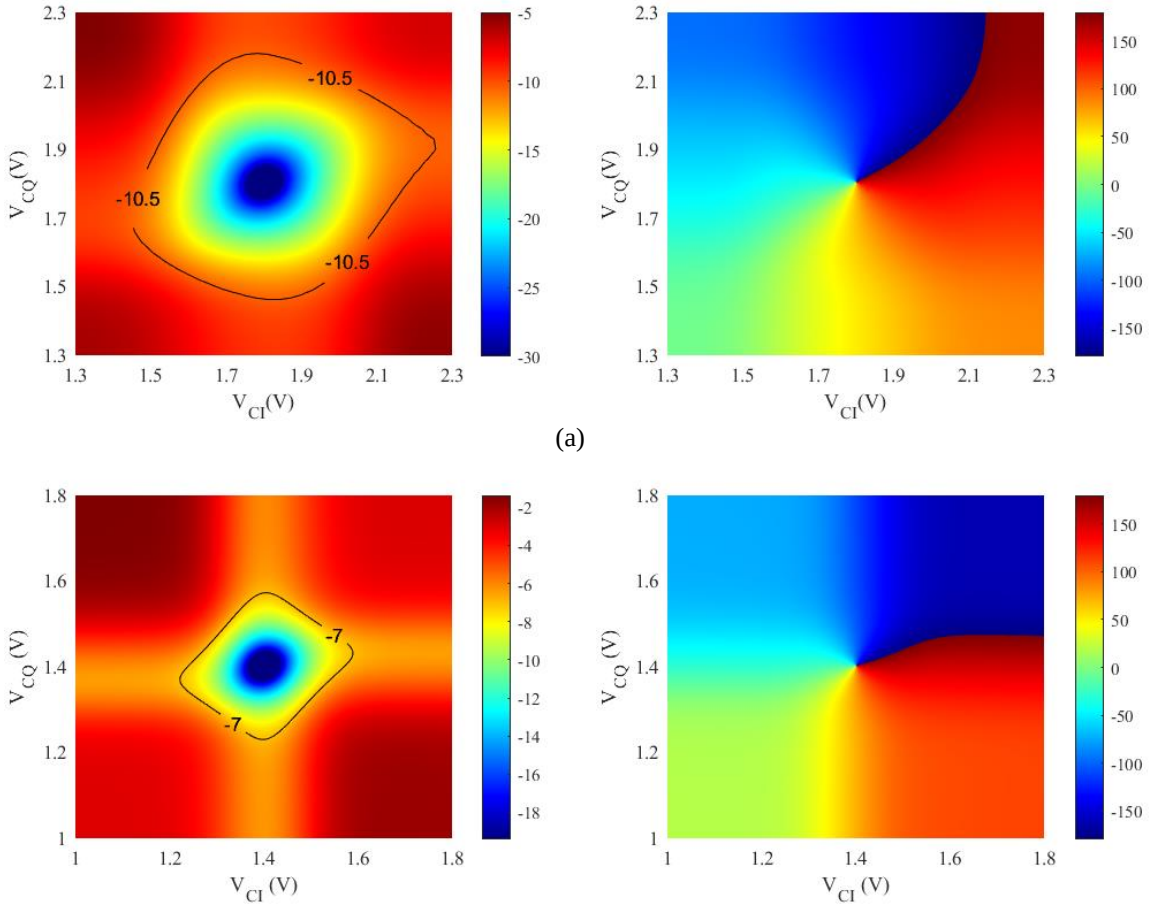


(a)



(b)

Fig. 3.11. Gain and insertion phase of the phase shifter as functions of control voltages V_{CI} and V_{CQ} for the corner cases of (a) ff, V_{DD} = 1.8 V, 90 °C and (b) ff, V_{DD} = 1.4 V, -30 °C at 28 GHz.



(a)

(b)

Fig. 3.12. Gain and insertion phase of the phase shifter as functions of control voltages V_{CI} and V_{CQ} for the corner cases of (a) ss, V_{DD}=1.8 V, 90 °C and (b) ss, V_{DD}=1.4 V, -30 °C at 28 GHz.

can be calibrated by tuning only V_{CI} and V_{CQ}. However, in some corner cases such as (ss, V_{DD} = 1.4 V, -30 ºC) and (ss, V_{DD} = 1.8 V, 90 ºC) where the maximum achievable constant gain is less than the one obtained in the nominal condition, as shown in Fig. 3.12, the circuit cannot compensate for the gain error unless additional gain tunability is provided for the circuit. In this work, to provide an additional adjustable gain, a variable resistor is used in the bias circuitry. By varying this resistor, the reference current is tuned and the consequently the bias points of the whole stages will be changed accordingly. Tuning this variable resistor adds up 4 dB of gain tunability to the phase shifter in this work. By increasing the reference current and tuning V_{CI} and V_{CQ}, the phase and gain errors are totally or partially (depending on the corner case) compensated.

The frequency response of 64 compensated phases and gains for the corners of (ss, V_{DD} = 1.4 V, -30 ºC) and (ss, V_{DD} = 1.8 V, 90 ºC) are shown in Fig. 3.13.

The frequency response of 64 corrected phases and gains for the corners of (ff, V_{DD} = 1.4 V, -30 ºC) and (ff, V_{DD} = 1.8 V, 90 ºC) are also shown in Fig. 3.14.

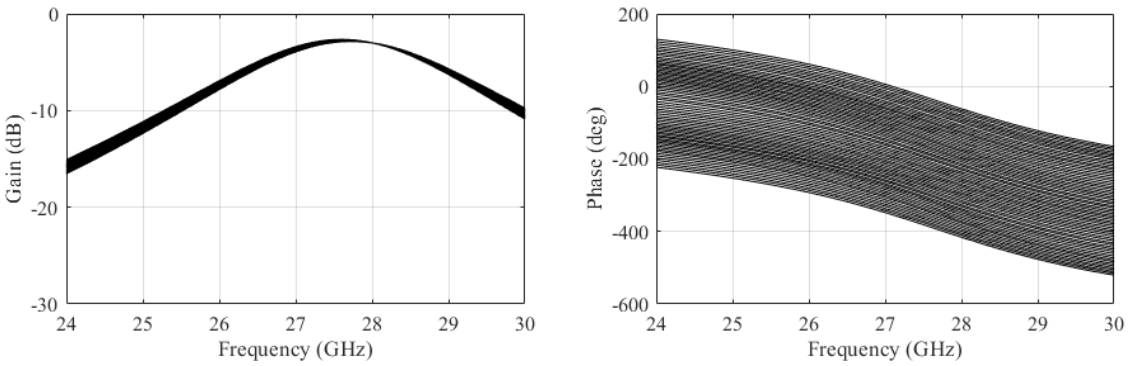
It is worth mentioning that in the phase shifter in this work, the variations in the center frequency of operation can be corrected by tuning the variable capacitors that are utilized at the output loads of the single-ended to differential signal converter and the phase shifter core.

In summary, based on the simulation results in Figs. 3.10–3.12, the phase shifter in this work can provide 360° of phase tuning with a constant insertion loss in the fast and slow process corners (ff and ss) as well as the nominal corner. The phase shifter's insertion loss at the fast process corner can remain equal to the insertion loss in the nominal corner given the supply voltage and temperature range of (1.4 V– 1.8 V) and (-30 °C– 90 °C), respectively. However, in the slow corner, the insertion loss increases by approximately 4 dB (compared to the nominal condition), and it is further increased for $V_{DD} \leq$ 1.6 V and $T \geq$ 27 °C, which may degrade the phase shifter's performance.

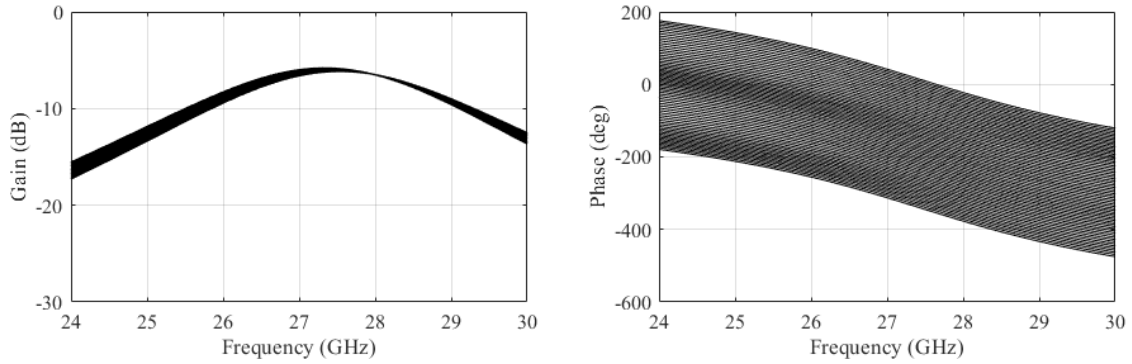
Monte Carlo simulations were also performed to examine the effect of local device mismatch (due to parametric process variations which mainly results in an imbalance of transistor geometry and threshold voltage) on the phase, gain, and bandwidth of the phase shifter. Based on the simulation results shown in Fig. 3.15, the standard deviation of the phase, gain, and bandwidth error for all 64 phase states are less than 1.63°, 0.3 dB, and 27.2 MHz, respectively. Standard deviation of phase error is well below the resolution of a 6-bit phase shifter (5.625º), which demonstrates that the designed phase shifter can properly operate as a 6-bit phase shifter.

Simulated noise figure of the phase shifter is better than 18 dB over the operation band.

The performance of the phase shifter is summarized and compared with several other RF phase shifters in Table 3.1. The phase shifter presented in this work provides 360^{o} of continuous phase tuning with an adjustable amplitude while consuming 27 mW of power and occupying 0.284 mm^2 of area (excluding the pads).

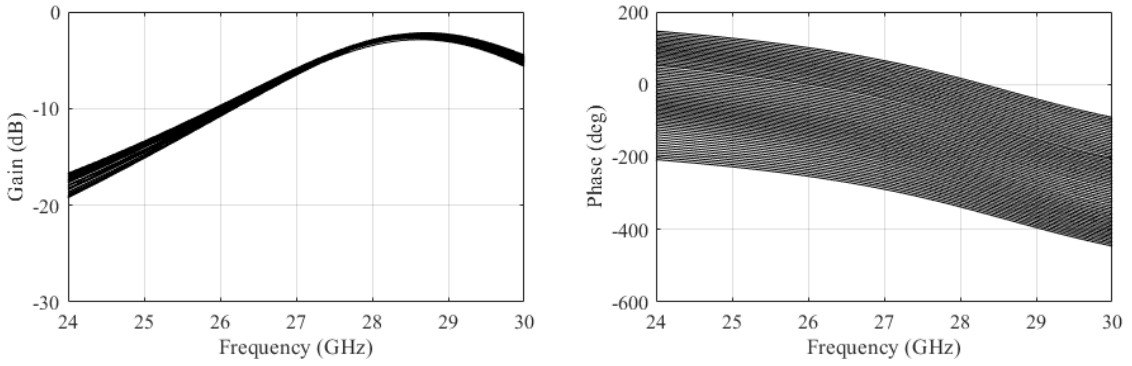


(a)

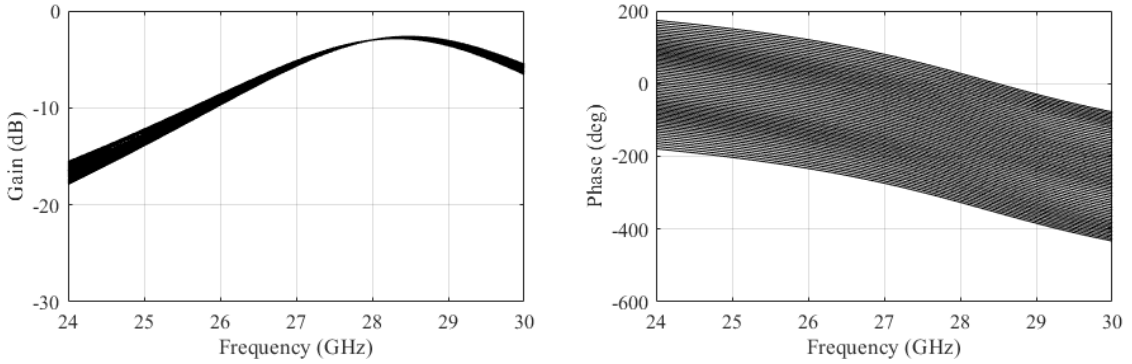


(b)

Fig. 3.13. (a) Frequency response of 64 corrected phases and gains for the corner of ss, V_{DD} = 1.4 V, -30 °C. 3-dB bandwidth=2.7 GHz. (b) Frequency response of 64 partially-corrected phases and gains for the corner of ss, V_{DD} = 1.8 V, 90 °C. 3-dB bandwidth=3.1 GHz.



(a)



(b)

Fig. 3.14. (a) Frequency response of 64 corrected phases and gains for the corner of ff, V_{DD} = 1.4 V, -30 °C. 3-dB bandwidth=3 GHz. (b) Frequency response of 64 corrected phases and gains for the corner of ff, V_{DD} = 1.8 V, 90 °C. 3-dB bandwidth=3.2 GHz.

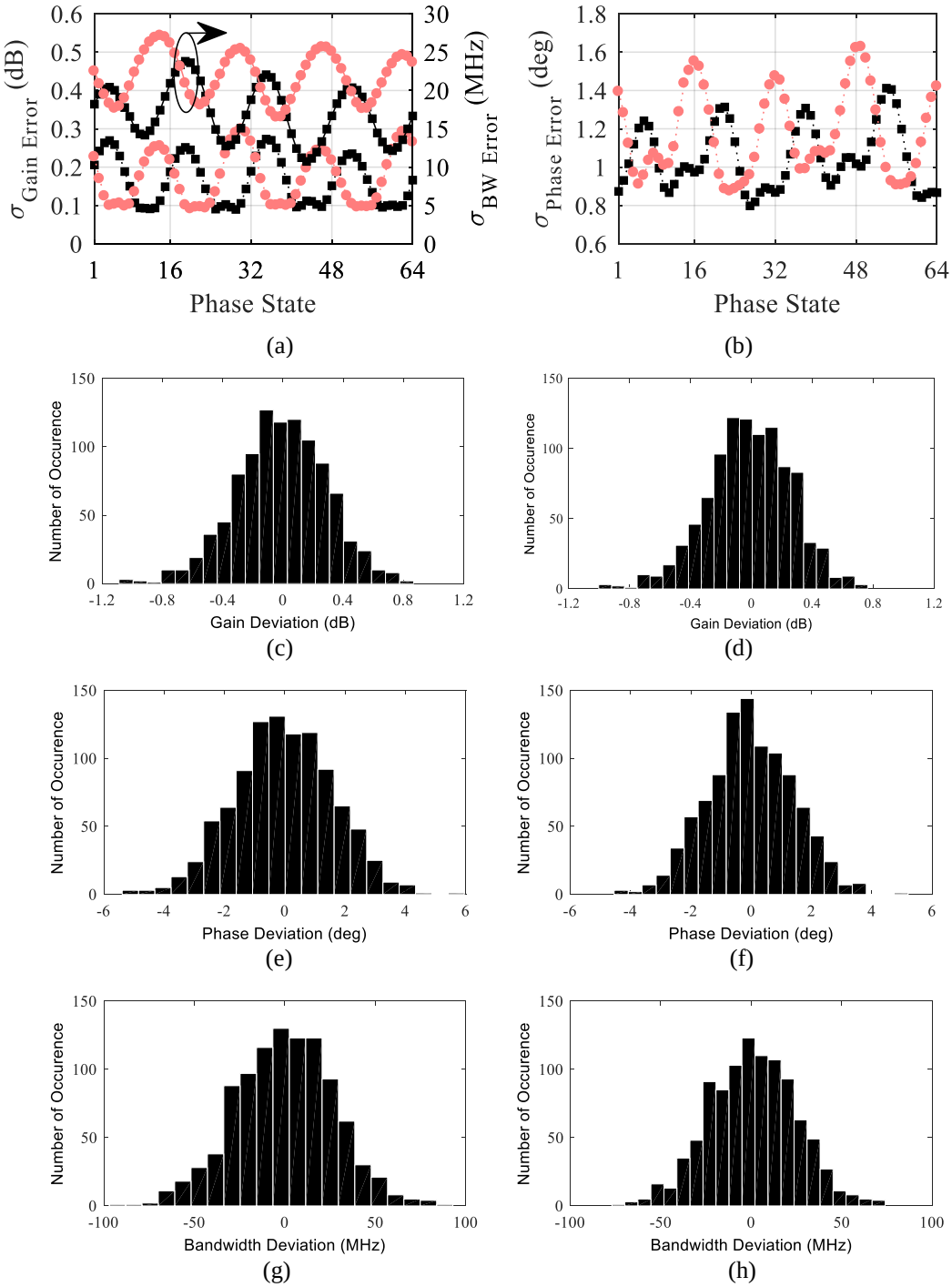


Fig. 3.15. Simulated standard deviation of (a) gain and bandwidth error and (b) phase error due to device mismatch for the phase shifter operating at the center frequency of 26 GHz (black squares) and 28 GHz (red circles). Monte Carlo simulations were performed with 1000 runs at each of the 64 phase states. Histogram graph of gain deviation for the case corresponding to maximum gain standard deviation at (c) 28 GHz and (d) 26 GHz. Histogram graph of phase deviation for the case corresponding to maximum phase standard deviation at (e) 28 GHz and (f) 26 GHz. Histogram graph of 3-dB bandwidth deviation for the case corresponding to maximum bandwidth standard deviation at (g) 28 GHz and (h) 26 GHz.

Table 3.1. Comparison table of RF phase shifters

Reference	This Work for f_c= 26GHz/28GHz	[46]	[33]	[47]	[54]	[55]	[56]	[57]	[58]
Process	130-nm CMOS	65-nm CMOS	180-nm CMOS	250-nm SiGe BiCMOS	130-nm CMOS	65-nm CMOS	65-nm CMOS	180-nm SiGe BiCMOS	65-nm CMOS
Frequency (GHz)	24.55–27.4[(1)] /26.55–29.4[(1)]	2–20	15–20	8–12	54-60	38-40	57–66	24	27.5−28.35
Phase Tuning Range	360°	360°	360°	360°	>90°	90°	360°	<300°	360°
Phase Resolution	Cont.	10-bit	Cont.	6-bit	Cont.	4º	6-bit	4-bit	4-bit
Gain (dB)	-6.1±1.5 /-4.95±1.5	-3.5±4.5[(4)]	-5±5	-4.5±2[(6)]	-7±0.7[(7)]	7.6±0.22[(8)]	-20±3	-13±2.6	-6.6±1
Power (mW)	27	92[(5)]	N/A	110	15.4	6.6	Passive	Passive	Passive
Area (mm^2)	0.284[(2)]/0.063[(3)]	2.16	0.722	1.646[(2)]	0.125[(3)]	0.161[(3)]	0.54[(2)]	0.365[(3)]	0.23[(3)]

[(1)]3-dB bandwidth [(2)]Excluding the pads [(3)]Phase shifter core [(4)]Estimated from the measured results [(5)]Excluding the buffer [(6)]Average gain [(7)]At 57 GHz [(8)] At 39 GHz.

3.4 Conclusion

A frequency tunable 360° analog CMOS phase shifter with an adjustable output amplitude has been presented. This phase shifter operates based on a vector summation technique and comprises of three stages including an active balun at the input and output and a phase shifter core which performs all the tasks of vector summation in a single block to save both the chip area and power consumption. The active baluns at the input and output of the phase shifter allow for single ended measurements and also provide input and output impedance matching, which enables operation of the phase shifter as a stand-alone IC. The phase shifter core includes an R-C PPF, generating quadrature signals, and several current steering variable gain amplifiers that are used to steer the quadrature currents in order to weight the amplitudes of the currents that are added at the output of the phase shifter core. This circuit allows for generating a signal with a tunable phase and amplitude while keeping the bias currents constant over the entire phase tuning range. This results in phase stability with respect to the input power level. The phase shifter has been designed and fabricated in 130-nm CMOS process. The chip occupies an area of 0.284 mm^2 (excluding the pads)

and consumes 27 mW of power. The center frequency of operation can be tuned within 26−28 GHz. The phase shifter's instantaneous 3-dB bandwidth is also 3 GHz. The phase shifter, which exhibits a negligible gain variation over the phase tuning range, is a good candidate for automotive radar as well as 5G applications.

Chapter 4: Scalable Phased Array Architectures with a Reduced Number of Tunable Phase Shifters

4.1 Introduction

A new architecture for scalable phased arrays is presented. In this architecture, a vector summation technique is used in a new RF feed network in order to reduce the number of tunable phase shifters in the phased array. In the new phased array architecture, one tunable phase shifter and N variable gain amplifiers adjust the signal phase and amplitude across the elements of an N-element subarray. The technique allows a number of subarrays to be connected (in a series or parallel configuration) to form a larger array providing a narrow beamwidth. This chapter introduces the proposed architecture and provides the analytical formulation of the vector summation applied to the array feed network. This formulation allows for array's optimal design through an optimization approach that maximizes scan range while limiting sidelobe levels and beamwidth. As a proof of principle, a four-element subarray is designed and its simulated performance is detailed.

An eight-element symmetric transmit phased array consisting of two four-element subarrays is also designed, fabricated, and tested at the Ku-band based on the described method. The design procedure as well as the measurement results for the eight-element phased array are presented. The eight-element phased array controlled by two phase shifters and eight variable gain amplifiers provides approximately 37^{o} of scan range.

Vector summation technique has been utilized in several phased array architectures to provide a tunable phase shift at each antenna port of the phased array [47], [59] –[61]. In this technique, the amplitude ratio of two vectors with a specific phase difference is adjusted to control the vector sum phase. Based on the published work, utilizing vector summation technique in phased arrays requires at least two variable gain amplifiers per antenna element to adjust the vector sum phase (through adjusting the relative amplitude of the two vectors) and vector sum amplitude (to provide the required excitation to antenna elements). Therefore, in arrays utilizing conventional vector summation techniques, for each antenna element, two vectors with a specific phase difference are needed where the phase and magnitude of their sum are tuned using at least two variable gain amplifiers. In contrast, in the circuit configuration introduced in this chapter, signal phase and amplitude along an N-element subarray are adjusted by employing N variable gain amplifiers and a single phase shifter (the phase shifter itself can be designed using a vector summation method). Therefore, the size and complexity of the phased array introduced in this chapter can be reduced as compared to other reported phased arrays employing vector summation technique [47], [59]–[61].

A variation of the described N-element subarray employing a single phase shifter and N number of variable gain amplifiers is also presented. In this variant, the number of active components and required control signals are reduced, resulting in further reduction of the array's complexity at the cost of reduced scan range. The simulated performance of an eight-element phased array including two four-element subarrays with the proposed configuration are also shown.

This chapter is organized as follows. Section 4.2 describes the architecture of the N-element subarray employing a single tunable phase shifter. Analysis of the N-element subarray is presented

in Section 4.3 followed by an optimum design procedure (based on particle swarm optimization algorithm) in Section 4.4. Simulation results showing the performance of a four-element subarray designed based on the particle swarm optimization algorithm are also presented in Section 4.4. Design of an eight-element phased array formed by two four-element subarrays is described in Section 4.5. Simulation and measurement results for the fabricated eight-element phased array operating over 12.4 –12.8 GHz are presented in Section 4.6. A similar phased array configuration with reduced number of both phase shifters and active components is also presented in Section 4.7, and the simulation results for an eight-element phased array designed based on the proposed approach are shown. Concluding remarks are presented in Section 4.8.

4.2 Description of the Phased Array Architecture with Reduced Complexity

The block diagrams of Fig. 4.1 illustrate the proposed N-element subarray. As shown in Fig. 4.1(a), the signal input to the transmit subarray is divided equally into two parts, one of which (S_{in1}) is phase shifted and injected into an N-way divider. The N-way divider outputs; b_1, b_2, …, up to b_N all have the same phase and magnitude. The other part (S_{in2}), is amplified by an amplifier having a voltage gain of A_1 and is added to b_1 using a combiner. Along the subarray, the complex signals (vectors) a_i and b_i (i = 1, 2, …, and N), are added together in the same manner. The amplitudes of the vector sums (i.e. a_i + b_i) are adjusted by using VGA_is whose outputs are themselves divided into two equal signals. One signal, denoted by e_i, feeds the ith radiating element, while the other signal is amplified by an amplifier with a voltage gain of A_{i+1} and added to b_{i+1}. Finally, the output of VGA_N is fed into the Nth radiating element (e_N). The phase of the vector sums a_i + b_i (i = 1, 2, …., and N) are determined by a_is' and b_is' relative amplitudes and phases. In order to control the array's beam, as the phase shifter is tuned, the gains of variable gain

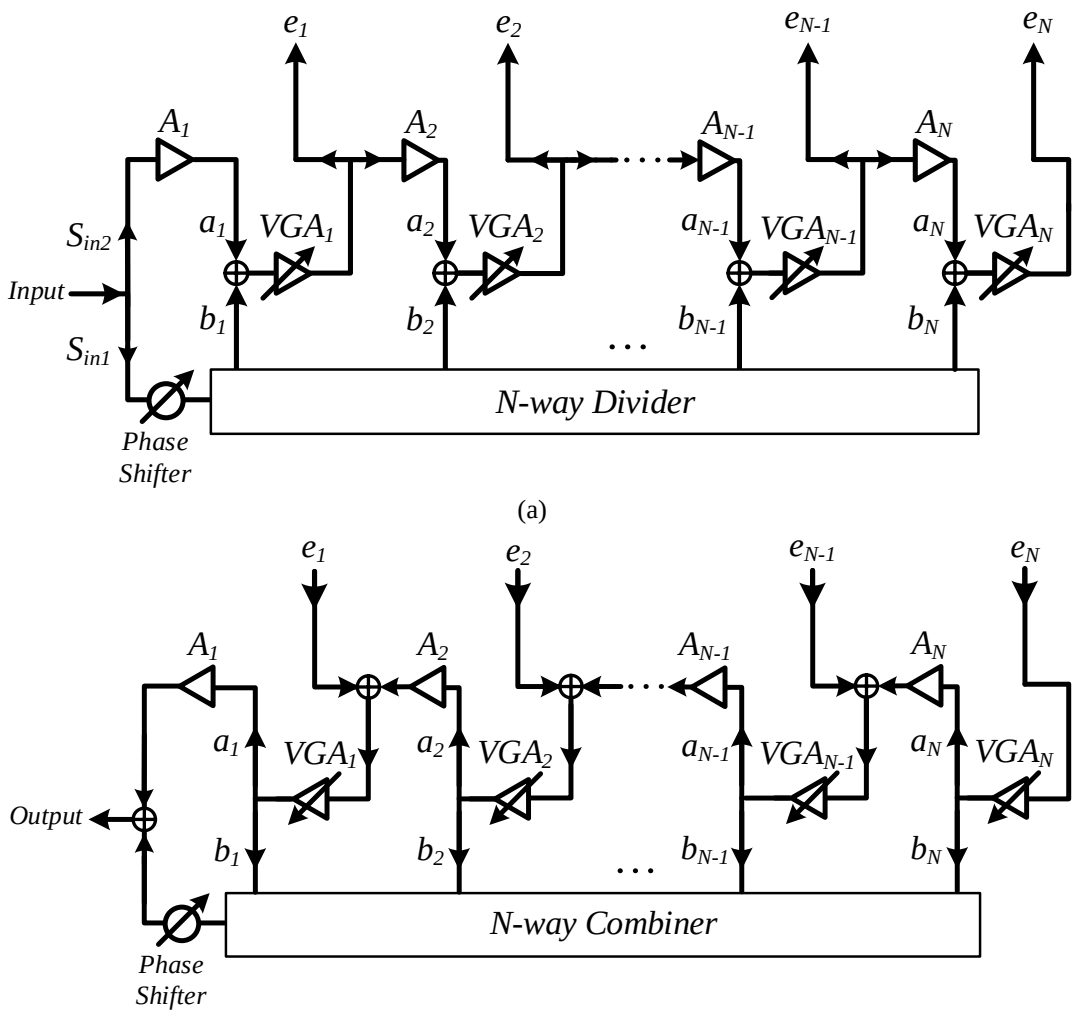


Fig. 4.1. Block diagram of the proposed approach for designing an N-element subarray with a single phase shifter. (a) Transmit mode. (b) Receive mode [62].

amplifier (VGA)s are also adjusted to provide the required antenna excitation phases and amplitudes along the array.

The architecture in Fig. 4.1(a) can be simply adapted for receive phased arrays by reversing the signal flow direction and interchanging the dividers and combiners, as shown in (b).

4.3 Analysis of the N-Element Subarray Employing a Single Tunable Phase Shifter

The circuit diagram for an N-element transmit subarray controlled by a single tunable phase shifter and N variable gain amplifiers is shown in Fig. 4.2. An N:1 two-way power divider is used

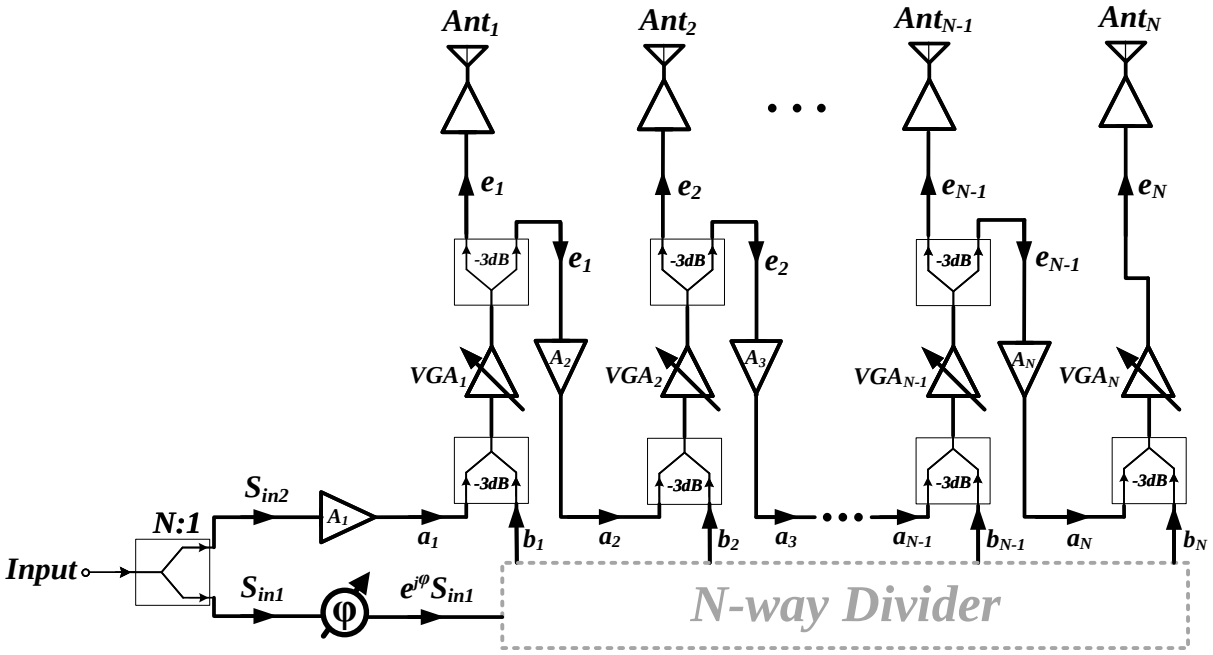


Fig. 4.2. The architecture of an N-element transmit subarray controlled by a single tunable phase shifter and N variable gain amplifier (VGA)s.

to divide the input signal into two parts, i.e. S_{in1} and S_{in2}, that are in phase while $|S_{in1}| = N^{1/2}|S_{in2}|$. The signal denoted by S_{in1} is phase shifted and fed to an N-way power divider which is designed to provide outputs with equal amplitudes and phases. Ideally, all b_is have a phase difference φ (generated by the tunable phase shifter) with respect to S_{in1} and S_{in2}. In this circuit, 3-dB power combiners are utilized to add the two vectors, a_i and b_i (i = 1, 2, …, N) while 3-dB power splitters are used to divide the output of VGA_is into two equal parts. Assuming a zero insertion phase for the gain blocks, divider/combiners, and interconnections, for now, the array output signals, e_i, are given by Eq. (4.1)

$$\begin{cases} e_1 = \dfrac{1}{2} VGA_1 (A_1 S_{in2} + b_1) \\ e_i = \dfrac{1}{2} VGA_i \left(A_i |e_{i-1}| e^{j\theta_{i-1}} + b_i\right) \quad (i = 2, \dots, \mathrm{N}-1) \\ e_N = \dfrac{1}{\sqrt{2}} VGA_N \left(A_N |e_{N-1}| e^{j\theta_{N-1}} + b_N\right), \end{cases} \tag{4.1}$$

where θ_i (i = 1, 2, …, N) is the phase of e_i, VGA_is denote the voltage gains of variable gain

amplifiers, b_is are equal to $S_{in2}e^{j\varphi}$, and A_is are constant voltage gains. According to Eq. 4.1, the magnitude of e_i is controlled by VGA_i. Assuming that S_{in2} has a magnitude of one and a phase of zero degree, θ_i (i = 1, 2, …, N) can be calculated as below

$$\begin{cases} \theta_1 = \tan^{-1}\left(\dfrac{\sin(\varphi)}{\cos(\varphi)+A_1}\right) \\ \theta_i = tan^{-1}\left(\dfrac{\sin(\varphi)+A_i\,|e_{i-1}|\sin(\theta_{i-1})}{\cos(\varphi)+A_i|e_{i-1}|\cos(\theta_{i-1})}\right) \quad (i=2,\dots,N) \end{cases} \tag{4.2}$$

Based on Eq. 4.2, phases of the signals exciting the antenna elements along the array are generally determined by the value of φ, A_is (i = 1, 2, …, N), and magnitudes of $e_i s$. The array's beam is controlled by adjusting gains of variable gain amplifiers as the phase shift φ is tuned. Here, for simplicity and without loss of generality, the phase shifter is assumed to have no insertion loss. However, for a lossy phase shifter having an amplitude loss of L_φ, the voltage gain of A_1 can simply be adjusted to A_1/L_φ so that Eq. 4.2 remains valid.

According to Eq. 4.2, when φ = 0°, e_is have equal phases, providing a broadside beam (scan angle = 0°). For φ > 0°, the phase progression of the signals along the array is ascending, which results in scan angles of less than 0°. The scan angle is greater than 0° for φ < 0° since the signal phase progression along the array is descending. When the sign of φ is inverted, the phases of $e_i s$ change sign as well. However, the magnitudes of $e_i s$ do not change (based on Eq. 4.1). Therefore, the sign of the scan angle is inverted, while the other features of the array's pattern remain the same.

4.4 Optimum Design Procedure for the N-element Subarray

The design goal for the N-element subarray in this work is to maximize the scan range for a given phase tuning range ($-\varphi_{max} \le \varphi \le \varphi_{max}$) while providing beamwidth and sidelobe levels

that are comparable to a uniformly-excited N-element phased array. To accomplish this, an optimization routine can be used to calculate the array parameters to achieve the design goals. The array factor is calculated as a function of φ, gains of A_is and variable gain amplifier (VGA_i)s. An optimization approach based on particle swarm optimization[2] introduced in [63], is utilized to determine the values for the array parameters to maximize the scan range. Particle swarm optimization has been utilized in the design of antennas and antenna arrays [64], [65] since it is a robust multidimensional optimization algorithm for finding the global maxima/minima in a complex problem (with multiple local maximums/minimums).

Here, particle swarm optimization is used to perform the following:

A. To find the optimum gains of A_is ($A_{i,opt}$s) and variable gain amplifiers ($VGA_{i,opt}$) that maximize achievable scan angle, given $\varphi = \varphi_{max}$.

B. Given the optimum constant gain values ($A_{i,opt}$s), found in part A, and a desired scan angle, to determine φ ($-\varphi_{max} < \varphi < \varphi_{max}$) and a gain value for each variable gain amplifier.

To perform the task A, scan angle for $\varphi = \varphi_{max}$ is defined as the cost function, which should be maximized. In each step of the optimization procedure, the values of variables A_is and VGA_is, are set by the optimization algorithm, and the array factor is calculated based on these values. If the beamwidth and sidelobe levels of the calculated array factor turn out to be comparable to a

[2] Particle swarm optimization algorithm is a multi-dimensional optimization routine that can optimize a function with multiple variables. Each variable should be given a specific range in which the optimal solution will be searched. The collection of the entire variables' ranges defines a multi-dimensional space. In this space, a number of agents, each showing one location (set of values for the variables), are selected. The ultimate goal of the optimization is to find the best location in the space, showing the optimum values for the set of variables, that maximizes or minimizes a predefined function which is called cost function. At the beginning of the optimization routine, the agents are randomly moved to search the entire space for the optimum values of the variables. In the optimization procedure, the agents are systematically moved toward personal best (pbest) and global best (gbest), where pbest is the best location of a specific agent throughout its entire previous movements, and gbest is the best location found by the entire agents (swarm). After completion of the algorithm, the gbest location is the global minimum/maximum of the cost function.

uniformly-excited phased array with the same number of elements, the scan angle can update the value of the cost function if it is larger than the cost function's current value.

To perform the task B, first, the constant gains of A_is are set to $A_{i,opt}$s found in part A. Then, M number of equally spaced scan angles, within the range 0–θ_{max}, are selected and denoted by θ_m, m = 1, 2, …, M, and the values of VGA_is and φ are optimized to generate a scan angle equal to (or with minimum error with respect to) θ_m. Here, the cost function is defined as the error between the achievable scan angle and θ_m, which should be minimized. In each step of the optimization procedure, the values of the variables φ and VGA_is are set by the optimization algorithm, and the array factor and corresponding scan angle are calculated. If the beamwidth and sidelobe levels of the calculated array factor turn out to be comparable to a uniformly-excited phased array with the same number of elements, the scan angle can update the value of cost function if it is smaller than the cost function's current value. (MATLAB codes that utilize particle swarm optimization algorithm to perform tasks A and B are provided in Appendix II.)

As an example, a four-element subarray is designed using the described optimization procedure. The optimization goals are set such that the array's half-power beamwidth is comparable to a uniformly-excited four-element array (with less than 10% error) while the sidelobe levels are kept below -11 dB (theoretical sidelobe level for a four-element uniformly-excited array is -11.3 dB). The variation range for φ is set to -170^o to 170^o.

Based on the optimization results, the maximum achievable scan angle of 32.5^o is obtained by setting the voltage gains $A_{i,opt}$s (i = 1, 2, 3, and 4) to 6.41, 1.31, 0.16, and -1.08, respectively ($A_{4,opt}$ is an inverting gain).

Fig. 4.3 shows the optimum values for φ and gain of each variable gain amplifier generating scan angles within the range -32.5^o to +32.5^o (maximum of 65° scan range). As shown in Fig. 4.3,

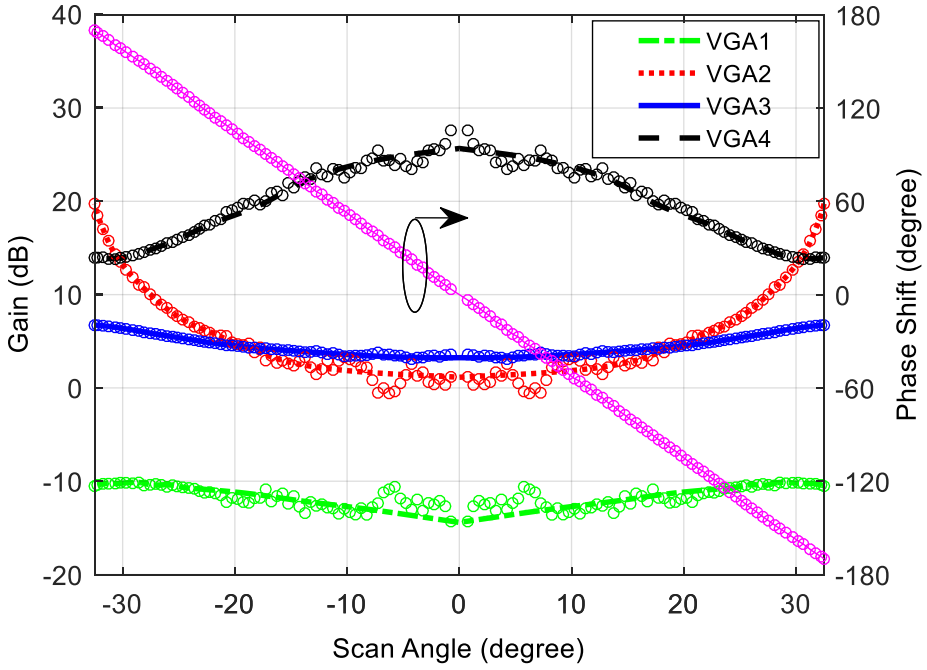


Fig. 4.3. Optimized values for ϕ and optimized and interpolated values for voltage gains of variable gain amplifier (VGA)s versus scan angle (circles: optimized values).

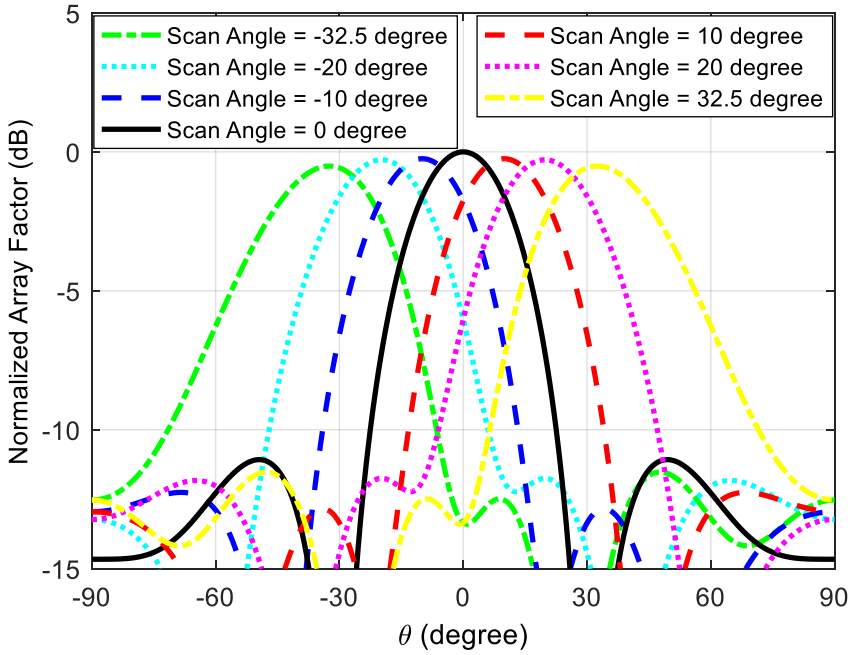
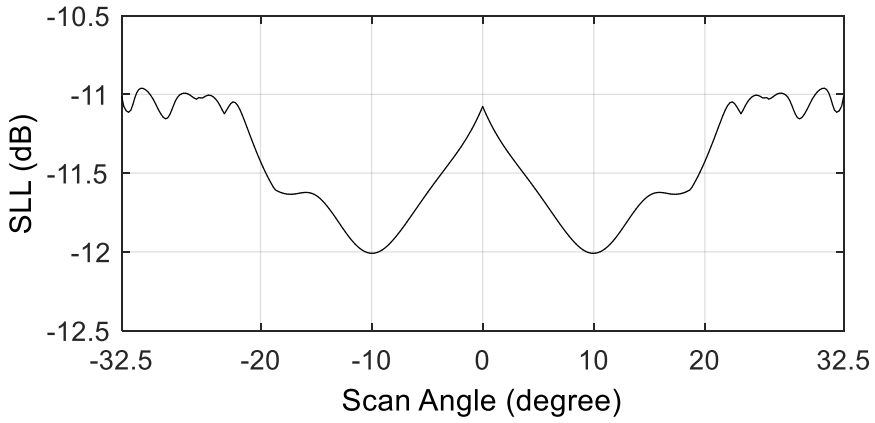


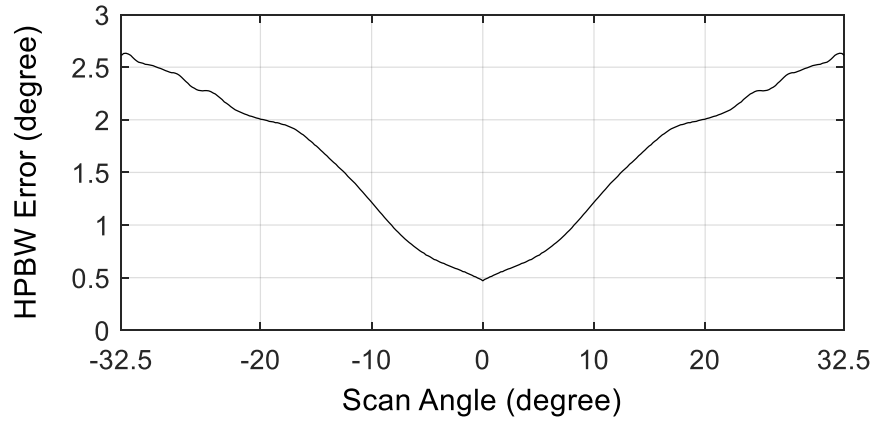
Fig. 4.4. Array factor of the four-element subarray at different scan angles.

scan angle varies approximately linearly with φ. However, it is observed that the optimized gain of the variable gain amplifiers do not vary monotonically versus scan angle. Since it is desirable to make the gain variation of the variable gain amplifiers a monotonic function of scan angle,

thereby simplifying their control circuity, a spline interpolation is applied to the optimization results for the gains of variable gain amplifiers, and the interpolated values are also shown in Fig. 4.3. The array factor for the subarray at different scan angles is shown in Fig. 4.4. As can be seen, the array gain is relatively constant over the entire scan range. The sidelobe level versus scan angle is shown in Fig. 4.5(a). Fig. 4.5(b) compares the absolute value of the difference between half-power beamwidth for the four-element subarray and that of a uniformly-excited four-element array at the same scan angle. This difference is denoted by half-power beamwidth (HPBW) error. The results shown in Fig. 4.5(a) and (b) confirm that after interpolating the gains of variable gain amplifiers, the specified optimization goals are still satisfied.



(a)



(b)

Fig. 4.5. (a) Sidelobe level (SLL) of the four-element subarray versus scan angle. (b) The difference between the half-power beamwidth of the four-element subarray and that of a uniformly-excited four-element array with the same scan angle (HPBW error).

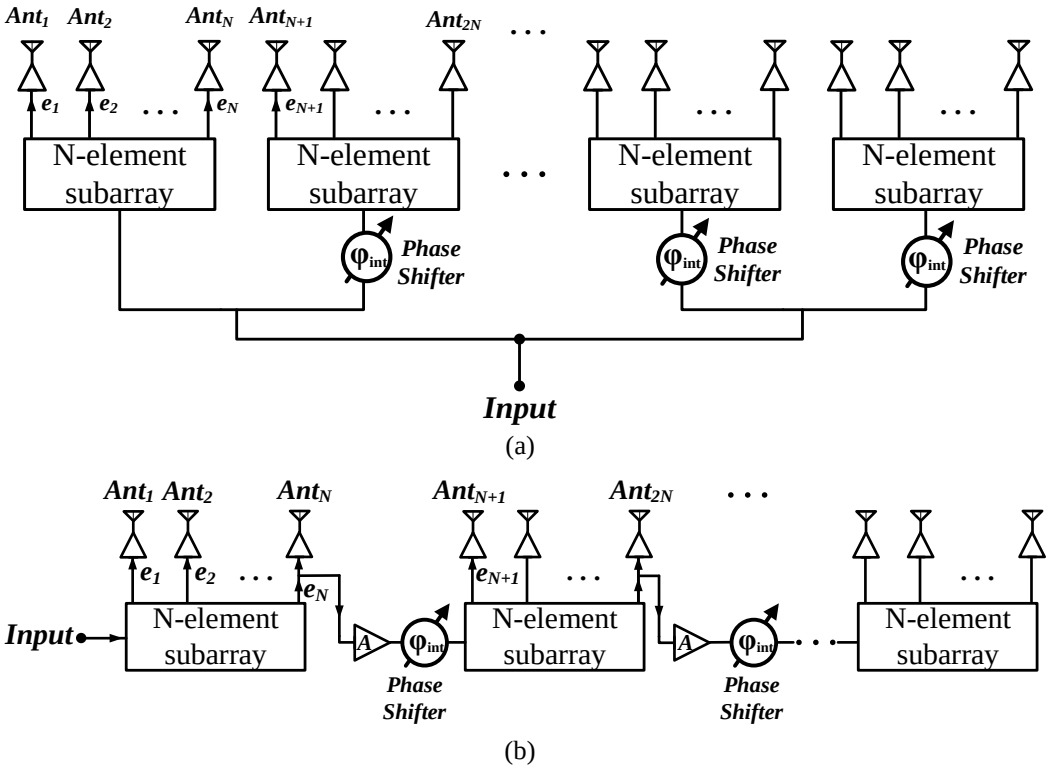


Fig. 4.6. (a) The structure of a large phased array that is formed by connecting N-element subarrays in parallel. (b) The structure of a large phased array that is formed by serially connecting N-element subarrays.

In general, the scan range for the described circuit decreases as the subarray size (number of elements) increases. This is due to the fact that the excitation phases of the antenna elements across the subarray are derived from a single phase shifter in the feed network.

To increase the array size while maintaining the scan range, a number of subarrays can be connected in parallel or series to form a larger array, as shown in Fig. 4.6. In this case, tunable phase shifters denoted by φ_{int} (in Fig. 4.6) are inserted to maintain the correct phase progression among the subarrays.

In this work, an eight-element symmetric phased array is designed and fabricated at Ku-band by using two four-element subarrays.

The eight-element phased array, described in Section 4.5, is controlled by two tunable phase shifters and eight variable gain amplifiers. Multiple eight-element phased arrays can be connected in series or in parallel (using the configurations shown in Fig. 4.6) to form a larger phased array.

4.5 Design of an Eight-Element Phased Array Employing Two Four-Element Subarrays

The circuit diagram for the eight-element symmetric phased array, designed at the Ku-band, is shown in Fig. 4.7. The input signal is equally divided between two subarrays by utilizing a Wilkinson power divider. A number of branch-line couplers with different coupling factors are used to form the main divider in the circuit. The coupling factor for each branch-line coupler is noted in Fig. 4.7. The Wilkinson power combiner/dividers used in Fig. 4.7 are all 3 dB splitters.

Hittite HMC-932LP4E is selected as a phase shifter for the circuit due to its minimal insertion loss variation versus phase shift. For variable gain amplifiers, MACOM MAAM-011100 is selected due to its compact size as well as small insertion phase variation versus gain. The S-parameters of HMC-932LP4E and MAAM-011100 were measured and the obtained data were used in circuit simulations. Based on the measured data, the phase shifter provides -170^o to 170^o phase shift, by tuning its control voltage from 0.08 V to 9.47 V. Furthermore, the gain of the variable gain amplifier can be tuned from -24.3 dB to +7.9 dB when its control voltage is varied from -1.95 V to 0 V.

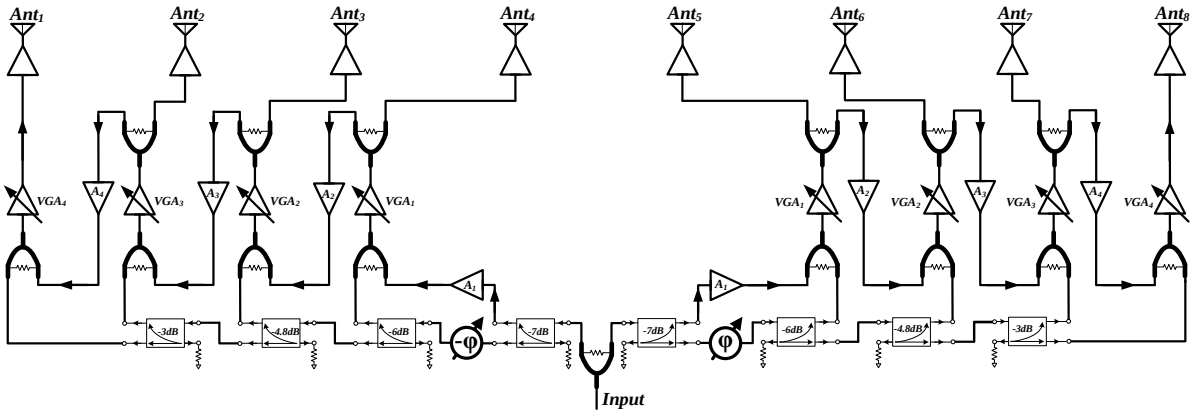


Fig. 4.7. Circuit diagram for an eight-element symmetric phased array consisting of two four-element subarrays [62].

Particle swarm optimization algorithm is used to find the $A_{i,opt}$s (i = 1, 2, 3, and 4) that maximize the scan range given -170° ≤ φ ≤ 170° while variable gain amplifiers operate within their measured tunable gain range. As a part of the design criteria, the sidelobe levels are kept below -12.5 dB while the array's half-power beamwidth has less than 10% error as compared to a uniformly-excited array of the same size. Based on the optimization results, the maximum achievable scan range is 42° (±21°) and $A_{i,opt}$s (i = 1, 2, 3, and 4) are equal to 1.42, 2.11, 0.74, and -1.85 respectively ($A_{4,opt}$ is an inverting gain). Furthermore, particle swarm optimization was used to generate the values for the phase shifts and gains of the variable gain amplifier

resulting in different scan angles. To simplify the control of the phased array, the gains of the variable gain amplifiers obtained through optimization are interpolated such that their values are monotonic functions of scan angle.

4.6 Simulation and Measurement Results

To simulate the circuit shown in Fig. 4.7, the de-embedded S-parameters of the variable gain amplifier MAAM 011100 and the phase shifter HMC 932LP4E are used in Keysight Advanced Design System (ADS) simulator. The passive components (couplers, Wilkinson power divider/combiners, and transmission lines) are simulated using ADS momentum and their S-parameters are imported to the schematic environment of ADS. In the final simulation, all the losses of the transmission lines, insertion phases of divider/combiners and interconnections, the insertion phases of the gain blocks as a function of their gains, the insertion losses of phase shifters as a function of their phase shifts, and the finite input and output return losses of all components have been accounted for.

The gains and phase shifts values are tuned to maximize the scan range while the main optimization goals specified before are satisfied over the scan range. The final values for A_1, A_2,

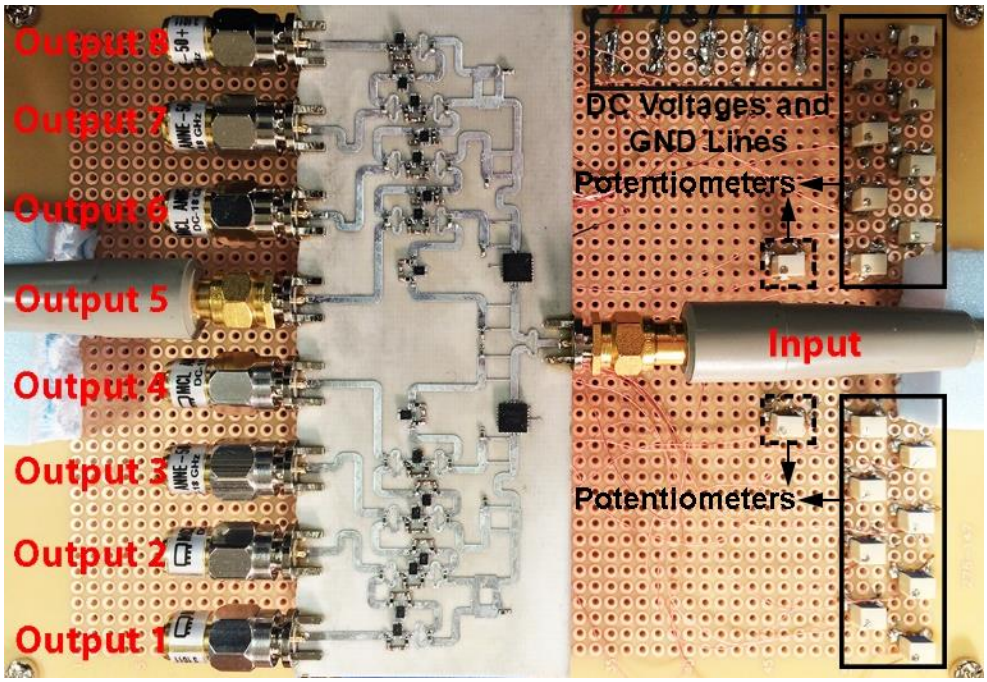


Fig. 4.8. Photograph of the fabricated eight-element phased array [62].

A_3, and A_4 are respectively equal to 1.64, 2.45, 0.7, and -1.76. The inverting gain A_4 is realized by connecting one MAAM-011100 amplifier to a half-wavelength transmission line (at the center frequency of operation).

Fig. 4.8 shows the photograph of the fabricated eight-element phased array on Rogers RO4003 substrate with thickness of 20 mils. In this circuit, the spacing between the output ports is half-wavelength (in free pace) at the center frequency of operation (12.6 GHz). The bias voltages for gain blocks (MAAM-011100) are V_D = +5 V, and V_G = -0.5 V provided by the dc voltage lines as shown in Fig. 4.8. The control voltages for the variable gain amplifiers vary from -1.01 V to -0.19 V. The control voltages for the phase shifters (Hittite HMC932LP4E) vary from 0.08 V to 9.47 V. The required control voltages for the gain blocks and the phase shifters are generated by using potentiometers connected to the dc voltage lines as shown in Fig. 4.8. The gain blocks are connected to the transmission lines by dc-decoupling capacitors. Furthermore, the phase shifters have internal dc-decoupling capacitors. The phased array circuit is stable at all frequencies.

In measurements, to steer the array's main beam, the control voltage of the phase shifters and variable gain amplifiers are initially set to the original values used in the circuit simulations. The array S-parameters are measured between the input port and each of the antenna ports (using a vector network analyzer) while the rest of the output ports are terminated with 50 Ω loads. Based on the measured S-parameters, the array factor is then calculated using a MATLAB code. The control voltage of the phase shifter is tuned to adjust the scan angle. Control voltages of the variable gain amplifiers are also tuned to adjust the half-power beamwidth and sidelobe levels. Each set of control voltages for phase shifters and variable gain amplifiers correspond to specific phase shift and gain values (considering the measured S-parameters for Hittite HMC932LP4E phase shifter and MACOM MAAM-011100 variable gain amplifier). Fig. 4.9 and Fig. 4.10 show the comparison between the measurement and circuit simulation results for φ and voltage gains of variable gain amplifiers versus scan angle, respectively. As shown in Fig. 4.9, the achievable scan range is 40^o ($\pm 20^o$) in the simulation results while the measured scan range is 36^o (from -18^o to $+18.5^o$). The simulated variation range for the gains of variable gain amplifiers is less than 13 dB which is very close to the measured gain variation range for variable gain amplifiers (14 dB) as shown in Fig. 4.10.

The simulated and measured array factors at 12.4 GHz, 12.6 GHz, and 12.8 GHz are compared in Fig. 4.11(a) and (b). The simulated array factors for scan angles of 0^o, $\pm 10^o$, and $\pm 20^o$ are shown in Fig. 4.11(a). The measured array factors corresponding to scan angles of 0^o, $\pm 10^o$, -18^o, and $+18.5^o$ are shown in Fig. 4.11(b). The simulated and measured sidelobe levels are less than -11.4 dB and -9 dB, respectively, over the band 12.4–12.8 GHz. In general, serially fed arrays exhibit frequency scanning (beam squint). By using symmetrically connected serially-fed arrays, this issue is largely addressed [66]. Furthermore, one can use several different negative group delay circuits

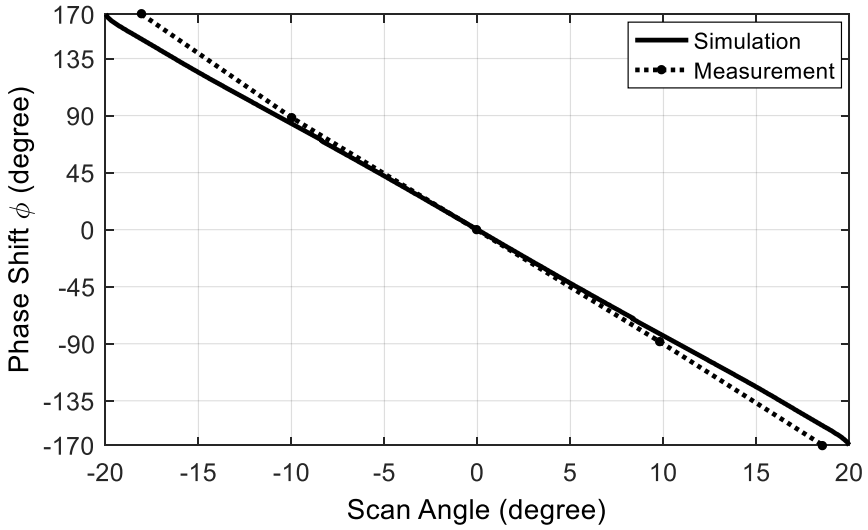


Fig. 4.9. Simulation and measurement results for ϕ versus scan angle.

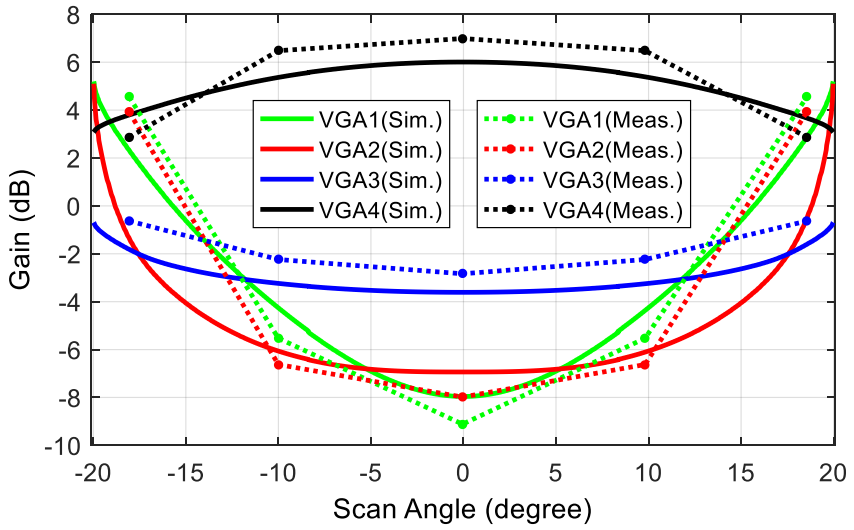
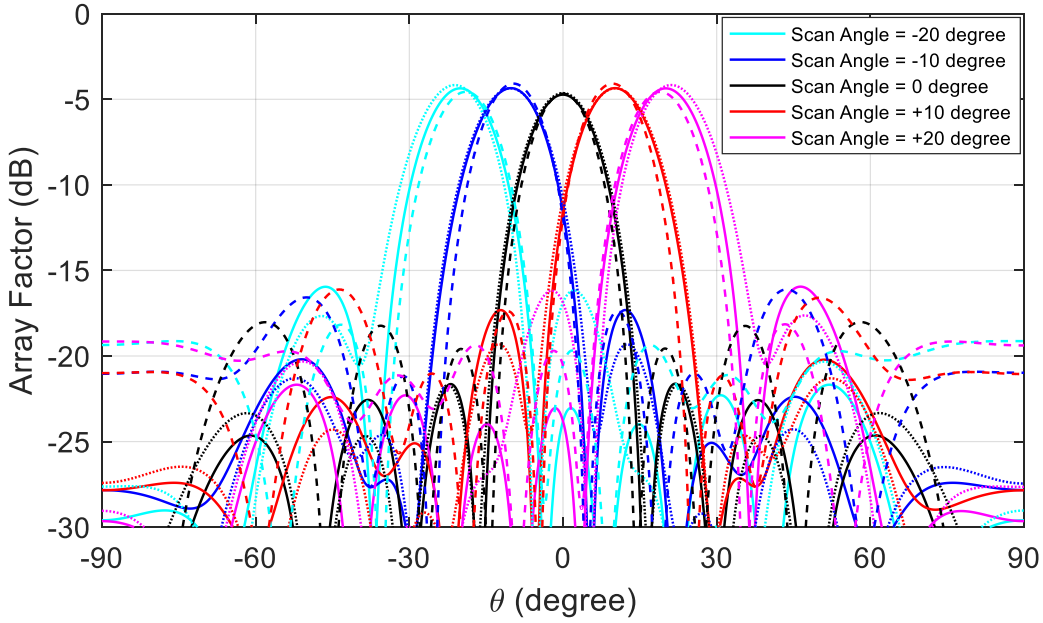
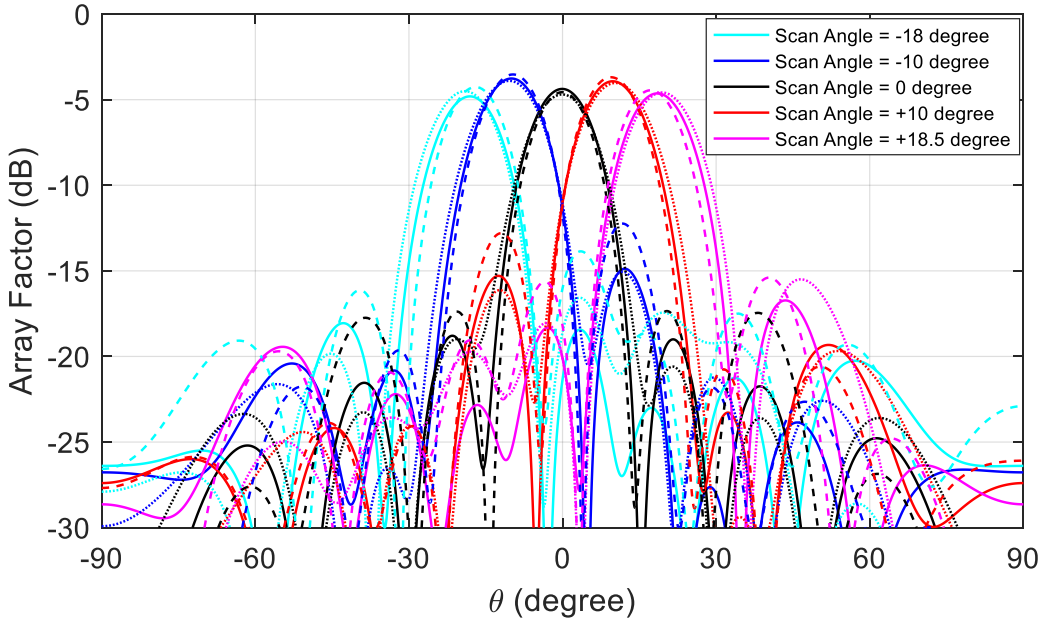


Fig. 4.10. Simulation and measurement results for the voltage gains of variable gain amplifier (VGA)s versus scan angle.

reported in the literature [67] –[69] to reduce or eliminate frequency scanning in serially fed phased arrays. In this work, the beam squint is less than ±1° within the range 12.4–12.8 GHz. It should also be noted that the array factor at the scan angle of 0° is slightly smaller than the array factor at other scan angles (Fig. 4.11). This is due to the fact that the gains of the variable gain amplifiers were approximated through an interpolation (applied to the optimized gain values obtained by using particle swarm optimization).



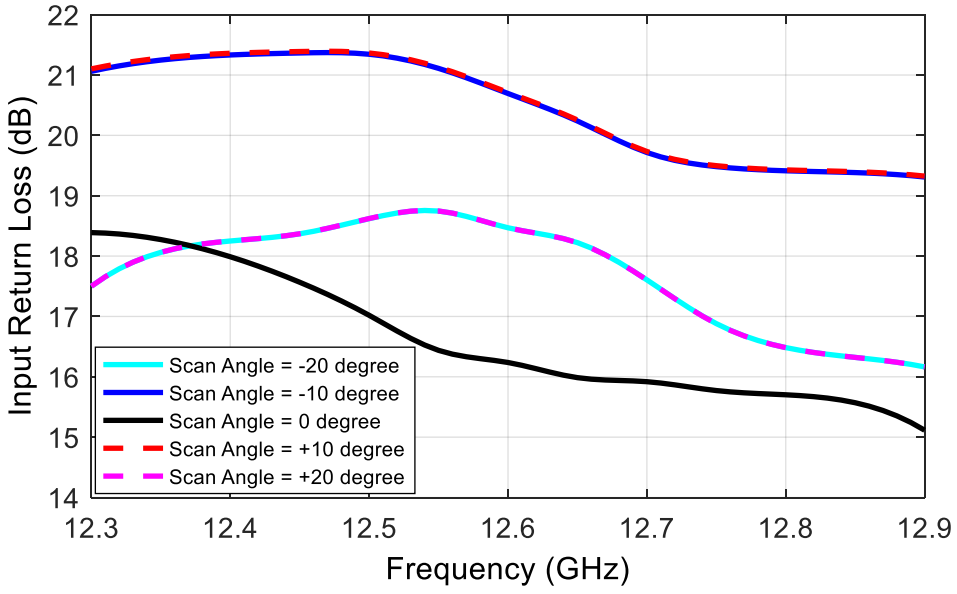
(a)



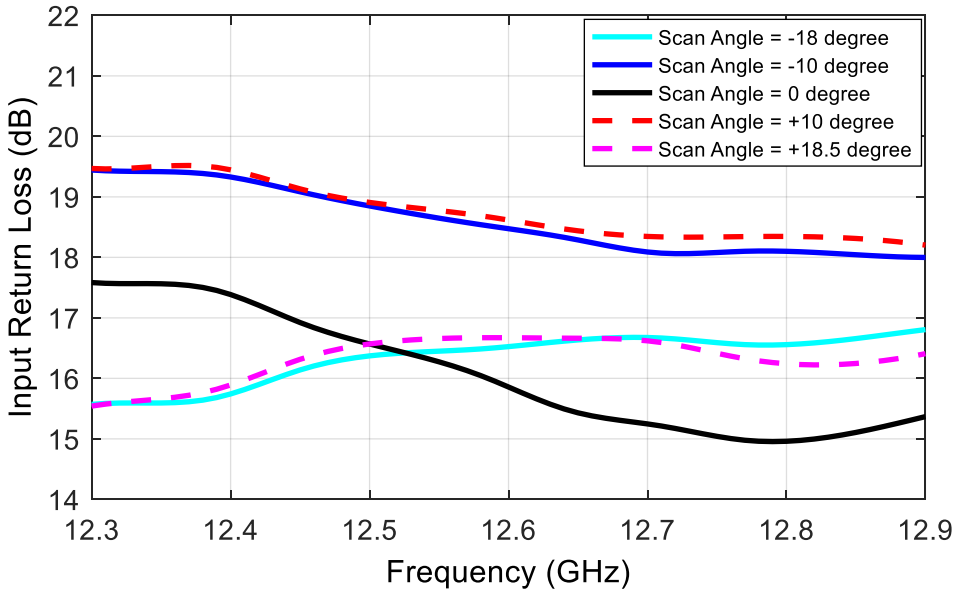
(b)

Fig. 4.11. Array factor for the eight-element phased array. (a) Simulation results. (b) Measurement results. (12.4 GHz: dotted line, 12.6 GHz: solid line, and 12.8 GHz: dashed line).

The simulated and measured input return loss of the eight-element phased array (for the same scan angles as in Fig. 4.11) are shown in Fig. 4.12(a) and (b), respectively. As can be seen, the simulated and measured input return loss are larger than 15 dB for any scan angle.



(a)



(b)

Fig. 4.12. Input return loss vs. frequency for the eight-element phased array. (a) Simulation results. (b) Measurement results.

As mentioned before, the array was characterized at each port while other ports were terminated with matched loads. The effect of coupling between array ports on its performance has also been investigated based on circuit simulations. The simulation results show that for the coupling levels of less than -10 dB between the adjacent ports (coupling phase was varied from -180^o to 180^o) the array's main beam deviates by less than 0.6^o while its beamwidth varies by 1.1^o

Table 4.1. Comparison between phased arrays with a reduced number of phase shifters

Reference	This work	[28]	[70]	[71]	[72]
Number of Elements	8	30	3x3	5	8
Number of Phase Shifters	2	12	4	2	2
Center Frequency (GHz)	12.6	7.9	28	77	2
Scan Range (degree)	37	28	29	16	25
Max. Sidelobe level (dB)	-9	-15	-9.5	-15	-10
Half-power Beamwidth	14.75	4.1	34	16	N.A.

as compared to the case where there is no coupling between the antenna ports. Furthermore, under this condition, array's sidelobe levels remain below -10 dB. It should be mentioned that often amplifiers are placed before the antennas in an array, which significantly reduces the effect of coupling on the weights of phased array elements.

The performance of the phase array presented in this chapter is summarized and compared with the published results from several recent phased arrays with a reduced number of phase shifters in Table 4.1. As compared to other phased arrays referenced in Table 4.1, the phased array in this work provides the largest value for scan range while having the smallest ratio of the number of phase shifters to the number of array elements.

4.7 Further Simplification of the Phased Array Architecture

It is possible to further reduce the phased arrays' front-end complexity through further reduction of the number of active components within the phased array, as shown in Fig. 4.13 [73]. This comes at the cost of reduced scan range and control over the array factor. The circuit architecture of Fig. 4.13 shows a variation of Fig. 4.1, where the excitation signal of the first antenna port is directly from the input signal of the subarray, while signals at other antenna ports are generated using a vector sum approach like the architecture of Fig. 4.1.

The operation of the new phased array is described here. A four-element subarray with the architecture of Fig. 4.13 is designed in ADS. The vector sum block S_i (i = 1, 2, and 3) has two

input vectors: a_i and b_i. The feed network is designed such that all b_is have the same magnitude (B) and phase while they have a phase difference of ϕ (generated by the phase shifter) with respect to the input signal. The signals denoted by a_is are generated by the constant gain stage, A_i, which amplifies the signal at the ith antenna port, E_i. Variable gain amplifiers are employed to equalize the magnitude of the signals at the antenna ports.

Considering the signal at the first antenna port, E_1, as a reference signal with a magnitude of one and a phase of zero degrees, the values of signals e_1 to e_4 are given by:

$$\begin{cases} e_1 = 1e^{j0} \\ e_i = VGA_{i-1}(Be^{j\varphi} + A_{i-1}e^{j\theta_{i-1}}), \quad (i = 2, 3, 4) \end{cases} \tag{4.3}$$

where θ_2 and θ_3 are phase of the excitation signals at the second and the third antenna ports, respectively, and are given by Eqs. (4.4) and (4.5).

$$\theta_2 = tan^{-1}\left(\frac{B_1\, sin(\Phi))}{(A_1 + B_1\, cos(\Phi))}\right) \tag{4.4}$$

$$\theta_3 = tan^{-1}\left(\frac{(A_2\, sin(\theta_2) + B_2\, sin(\Phi))}{(A_2\, cos(\theta_2) + B_2\, cos(\Phi))}\right) \tag{4.5}$$

Phase of the excitation signal at the fourth antenna port, θ_4, is given by Eq. (4.6).

$$\theta_4 = tan^{-1}\left(\frac{(A_3\, sin(\theta_3) + B_3\, \sin(\Phi))}{(A_3\, cos(\theta_3) + B_3\, \cos(\Phi))}\right). \tag{4.6}$$

Beam steering can be achieved by controlling only the phase shift φ while the gains of A_i (i = 2, 3, 4) are set to constant optimum values resulting in maximum scan range.

An eight-element symmetric phased array comprising of two identical four-element subarrays with the architecture of Fig. 4.13 is designed to operate within 12.4–12.8 GHz.

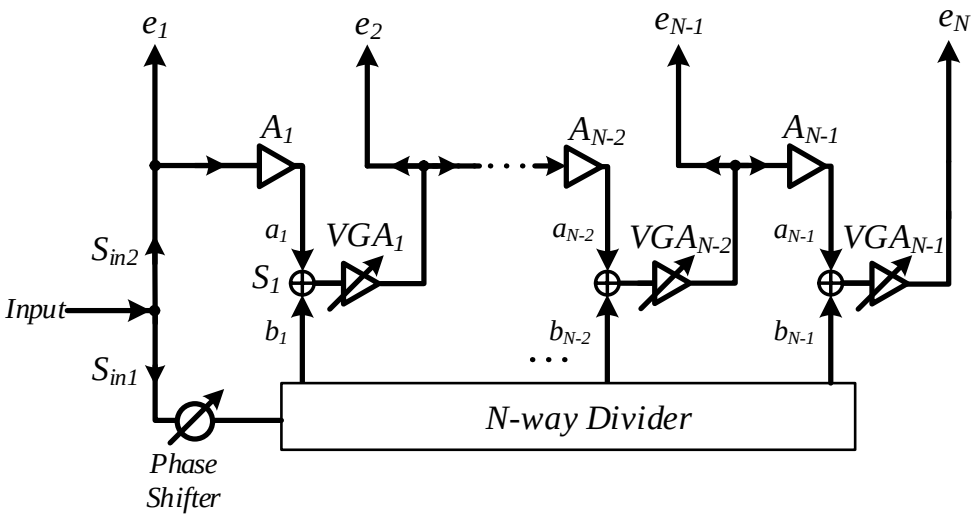


Fig. 4.13. Architecture of the proposed N-element subarray using a single phase shifter and (N-1) variable gain amplifier (VGA)s.

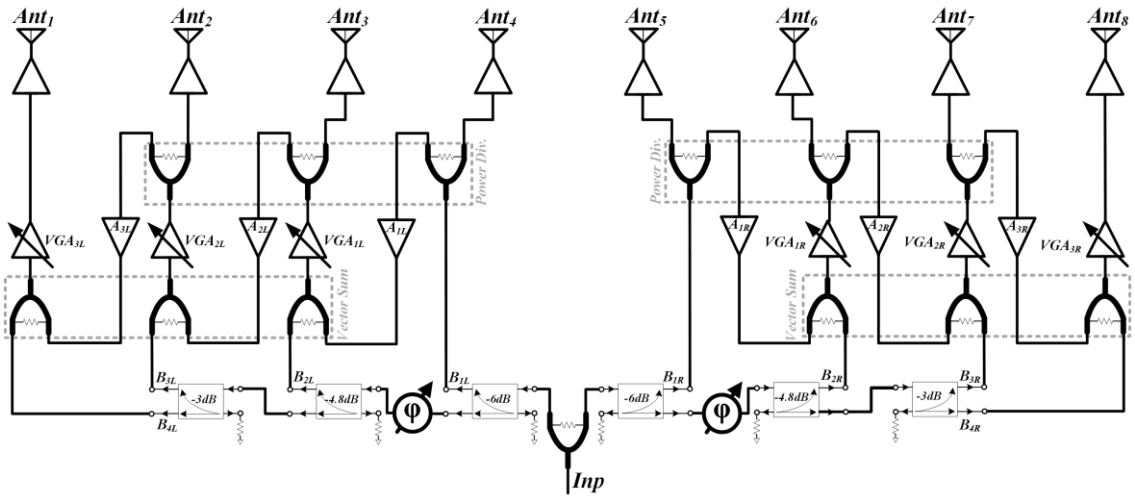


Fig. 4.14. Circuit diagram of the proposed eight-element phased array controlled by two phase shifters and six variable gain amplifiers.

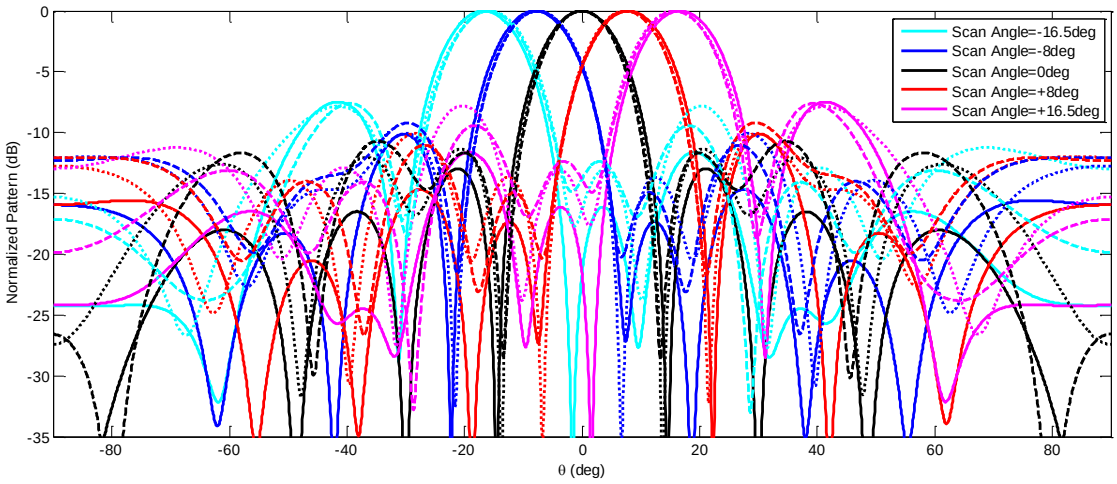


Fig. 4.15. Simulated normalized array factors for the eight-element array at 12.4 GHz (dotted line), 12.6 GHz (solid line), and 12.8 GHz (dashed line).

The phased array, shown in Fig. 4.14, is designed on a Rogers RO4003 substrate with 20 mil thickness. The utilized variable gain amplifiers are MACOM MAAM 011100 and the phase shifters are Hittite HMC 932LP4E.

Fig. 4.15 shows the simulation results for the normalized array factor of the phased array at 12.4 GHz, 12.6 GHz, and 12.8 GHz at various scan angles. The phased array provides 33° of scan range (from -16.5° to +16.5°). The beam squint is less than 1° within the scan range and the specified bandwidth (12.4–12.8 GHz). Simulation results show that sidelobe level is lower than -13 dB at broadside, and it approaches -7.2 dB at the scan angles of ±16.5 degrees. The main reason for degradation of sidelobe levels at higher scan angles is that the excitation phase of the signals at the fourth and fifth antenna ports (first antenna port in each subarray) are equal for all values of φ. Consequently, sidelobe level increases for higher scan angles. One can taper the magnitude of the signals at the antenna ports to achieve better sidelobe levels.

4.8 Conclusion

A new architecture has been devised for scalable phased arrays with reduced number of phase shifters. This architecture incorporates vector summation into a new feed network to adjust the signal phase distribution across the array elements with a reduced number of phase shifters. As a result, the presented phased arrays have less complexity and require fewer control signals as compared to the conventional phased array design approaches. An eight-element transmit phased array controlled by two tunable phase shifters and eight variable gain amplifiers has been designed, fabricated, and measured at the Ku-band. The measurement results show that the phased array provides approximately 37^{o} of scan range at the center frequency of 12.6 GHz. The measured input return loss is better than 15 dB and sidelobe levels are lower than -9 dB over the operation band and scan range. It is also shown that the presented phased array architecture with reduced number

of phase shifters can be further simplified through the reduction of the number of active components, but at the cost of smaller scan range. An eight-element phased array with reduced number of phase shifters and active components has been designed and its performance has been presented. The described phased array architectures are promising candidates for limited-scan applications where the major concern is the low-complexity of the system such as in long-range radars for automotive industry.

Chapter 5: A Low-Complexity Wide-Scan Integrated Phased Array

5.1 Introduction

In this chapter, a new circuit for a wide-scan, scalable, integrated phased array transmitter is presented. In this circuit architecture, the array's control complexity is reduced by decreasing the number of phase shifters and their associated control signals. To reduce the number of phase shifters, phase shifting function is integrated into the feed network of a scalable subarray by incorporating vector summation in the feed network. A number of subarrays can be connected to form a large array, providing a narrow beam.

As a proof of concept, an eight-element symmetric phased array comprised of two four-element subarrays is designed at K band and fabricated using 130-nm CMOS process. The phased array employs four phase shifters and provides ±15° of continuous scan range (which corresponds to an average inter-element phase difference of approximately ±45°) with less than -10 dB of sidelobe levels. The half power beamwidth has less than 5% error compared to the beamwidth of an eight-element uniformly-excited array with the same scan angle. To increase the scan range up to ±90° (corresponding to an inter-element phase difference of ±180°), a quadrature signal generator network in conjunction with quadrant selector switches are used at each channel. Here, the total number of phase shifters and their corresponding control signals are reduced by a factor of two as compared to conventional phased arrays which use one phase shifter per radiating element. The eight-element phased array provides ±90° of scan range with less than 15% of half

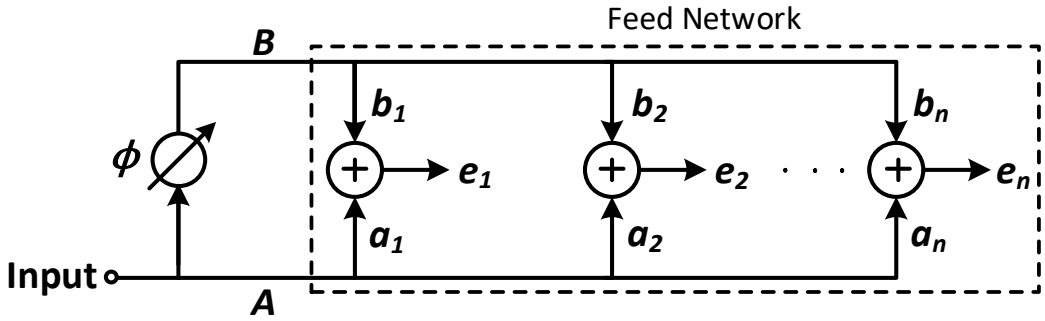


Fig. 5.1. Block diagram of a transmit subarray employing a single phase shifter.

power beamwidth error compared to an eight-element uniformly-excited array and sidelobe levels smaller than -9 dB while consuming 680 mW of dc power and occupying a chip area of 6.64 mm^2.

This chapter is organized as follows. The operation principle of the scalable subarray with reduced number of phase shifters is described in Section 5.2. Design of the wide-scan, scalable, eight-element phased array is presented in Section 5.3. Simulation and measurement results are provided in Section 5.4 followed by the discussion and conclusion in Section 5.5.

5.2 Operating Principle for the Low-Complexity Scalable Subarray

Block diagram of an $\boldsymbol{N}$-element transmit subarray employing a single phase shifter is presented in Fig. 5.1 [74]. In this architecture, the signal at each radiating-element ($\boldsymbol{e_i}$) is the vector-sum of two signal components, $\boldsymbol{a_i}$ and $\boldsymbol{b_i}$ ($\boldsymbol{i}$ = 1, 2, …, $\boldsymbol{N}$), generated by distributing the input signal through two feed networks with a phase difference of $\boldsymbol{\varphi}$ and unequal power distribution. Assuming a phase of zero degrees for $\boldsymbol{a_i}$s and a phase of $\boldsymbol{\varphi}$ for $\boldsymbol{b_i}$s, the phase and magnitude of the signal at the $\boldsymbol{i}$th radiating element, $\boldsymbol{e_i}$ ($\boldsymbol{i}$ = 1, 2, …, $\boldsymbol{N}$), are given by Eq. (5.1) and Eq. (5.2), respectively.

$$\angle \boldsymbol{e_i} = \tan^{-1}\left(\frac{\sin(\boldsymbol{\varphi})}{\left|\frac{\boldsymbol{a_i}}{\boldsymbol{b_i}}\right| + \cos(\boldsymbol{\varphi})}\right) \tag{5.1}$$

$$|\boldsymbol{e_i}| = \sqrt{(|\boldsymbol{a_i}| + |\boldsymbol{b_i}|\cos(\boldsymbol{\varphi}))^2 + (|\boldsymbol{b_i}|\sin(\boldsymbol{\varphi}))^2}. \tag{5.2}$$

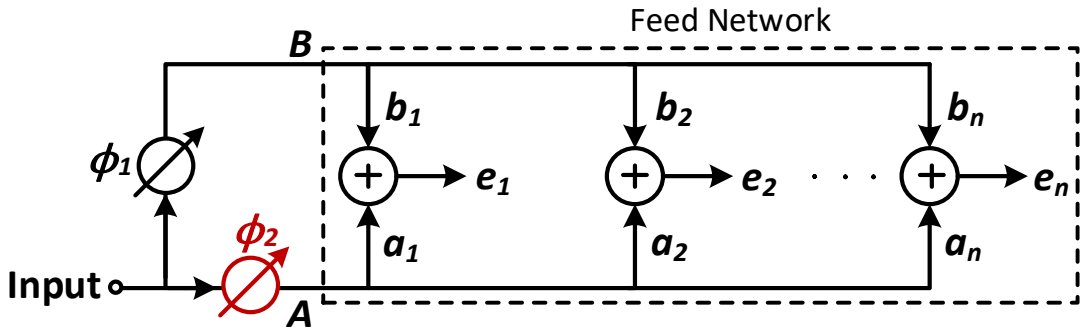


Fig. 5.2. Block diagram of the *N*-element scalable transmit subarray employing two phase shifters.

According to Eqs. (5.1) and (5.2), the signal phase and amplitude at each radiating element depends on the amplitudes of $|\boldsymbol{a_i}|$s and $|\boldsymbol{b_i}|$s as well as their phase difference ($\boldsymbol{\varphi}$). For a simple control of beamforming and beam steering, the amplitudes of $|\boldsymbol{a_i}|$s and $|\boldsymbol{b_i}|$s are set to be constant, while $\boldsymbol{\varphi}$ is varied to control the amplitudes and phases of $\boldsymbol{e_i}$s. The selected values for $|\boldsymbol{a_i}|$s and $|\boldsymbol{b_i}|$s highly impact the phased array's characteristics. In this work, $|\boldsymbol{a_i}|$s and $|\boldsymbol{b_i}|$s are optimized for the maximum scan range with limited sidelobe level and half power beamwidth.

It should be noted that since the excitation phases of the antenna elements across the subarray are derived from a single phase shifter, this phased array architecture provides a limited scan range, i.e. the scan range is reduced as the number of elements ($\boldsymbol{N}$) in this architecture increases. Based on the optimization results, the maximum achievable scan range with sidelobe levels smaller than -10 dB and half power beamwidth error of less than 5% (compared to a uniformly-excited array) is approximately ±9.5°, ±7°, ±5°, and ±4.5° for a four, six, eight, and ten element subarray. To increase the number of array elements (in order to provide a narrow beamwidth) while maintaining the scan range, several smaller subarrays must be employed to form a large phased array.

To design a scalable subarray, one phase shifter is added to the architecture of Fig. 5.1 as shown in Fig. 5.2. This extra phase shifter allows for maintaining correct phase progression among subarrays in a larger array formed by connecting several subarrays, as shown in Fig. 5.3.

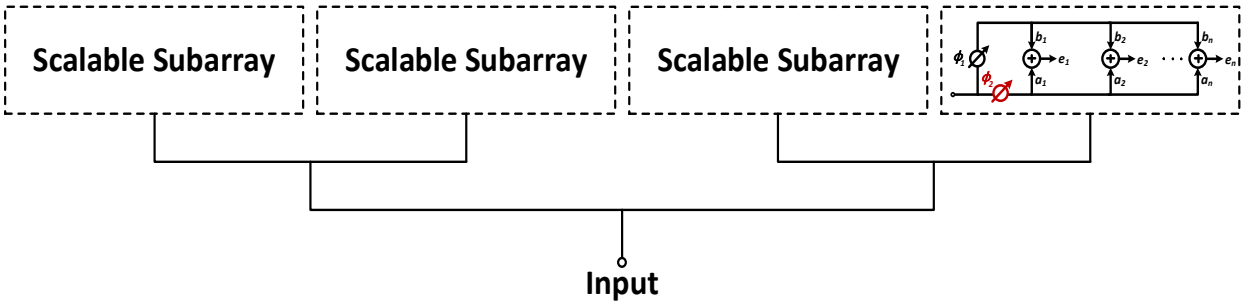


Fig. 5.3. Structure of a large phased array that is formed by connecting N-element scalable subarrays in parallel.

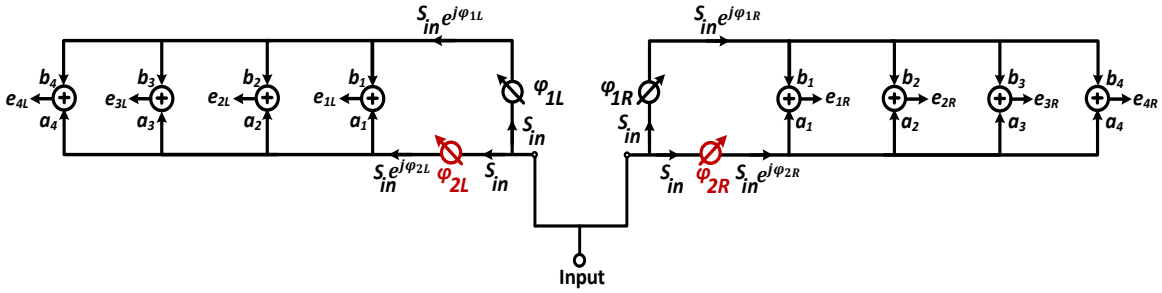


Fig. 5.4. Configuration of the eight-element phased array that is formed by symmetric connection of two four-element subarrays.

In this work, an eight-element phased array is formed by symmetric connection of two four-element subarrays, as shown in Fig. 5.4. To design the eight-element phased array for the maximum scan range while limiting sidelobe level and half power beamwidth, first, array factor is calculated as a function of the design parameters which are the weights of the signals with phases of $\boldsymbol{\phi_1}$ and $\boldsymbol{\phi_2}$. The array factor is given by Eq. 5.3.

$$AF = \sum_{k=1}^{k=4} e_{kR}\, e^{j(k-1)\pi \sin(\theta)} + \sum_{k=1}^{k=4} e_{kL}\, e^{j(8-k)\pi \sin(\theta)}, \tag{5.3}$$

where e_{kR} and e_{kL} (k = 1, 2, 3, and 4) represent the excitations of the right and left side four-element subarrays, respectively. The excitations of e_{kR} and e_{kL} are given by Eq. 5.4.

$$\begin{cases} e_{i,R} = |a_i|e^{j\varphi_{2R}} + |b_i|e^{j\varphi_{1R}} \\ e_{i,L} = |a_i|e^{j\varphi_{2L}} + |b_i|e^{j\varphi_{1L}} \end{cases}. \; i = 1, 2, 3, 4 \tag{5.4}$$

For the eight-element phased array in this chapter, a_3, b_3, a_4, and b_4 are set to be equal to b_2, a_2, b_1, and a_1, respectivley. By substituting Eq. (5.4) into Eq. (5.3), array factor will be a function of the signal weights ($|a_i|$ and $|b_i|$, i=1 and 2) and phases (φ_1 and φ_2). A particle swarm optimization routine is utilized to provide the optimum values of $|a_i|$ and $|b_i|$ (i=1 and 2) that allow for maximum scan range with limited sidelobe levels and half power beamwidth as the relative phase between the phase shifters (φ_2-φ_1) is varied. Based on the utilized optimization procedure, the optimum values of $|a_1|$, $|a_2|$, $|b_1|$, and $|b_2|$ which allow for maximum scan range with less than -10 dB of sidelobe levels are equal to 7, 8, 5, and 1 (normalized to the value of $|b_2|$),

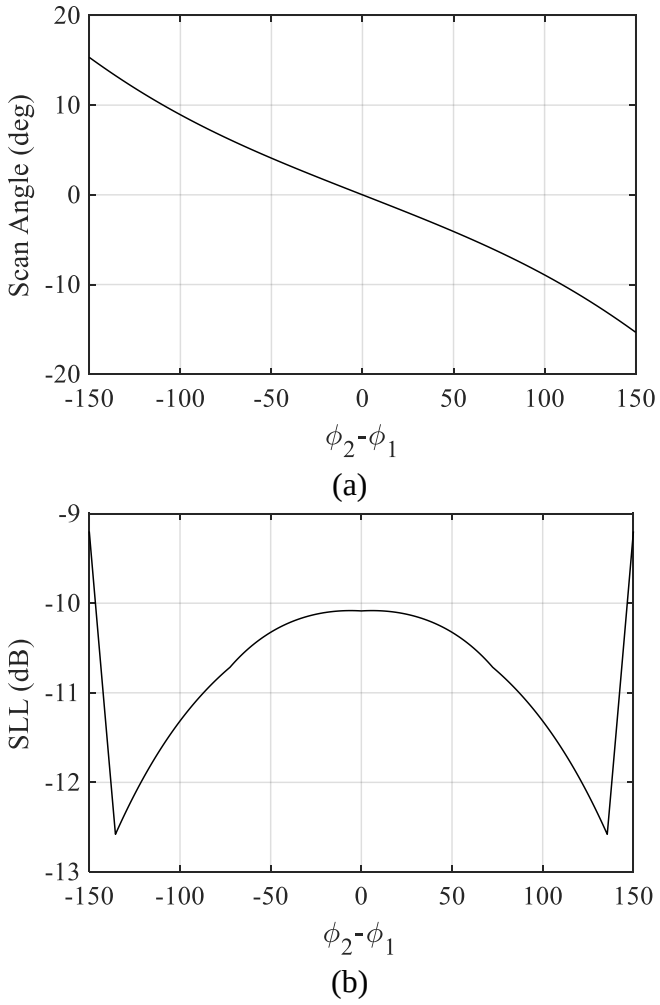


Fig. 5.5. (a) Scan angle and (b) sidelobe level (SLL) of the phased array discussed in this chapter.

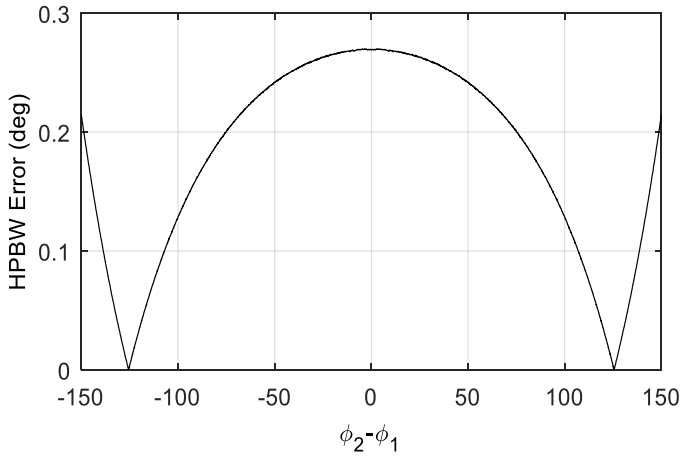


Fig. 5.6. The difference between half power beamwidth of the phased array discussed in this chapter and that of a uniformly-excited eight-element array with the same scan angle (HPBW error).

respectively. For the optimum values of $|a_1|$, $|a_2|$, $|b_1|$, and $|b_2|$, the scan range is from -15° to 15° and sidelobe levels are less than -10 dB for $|\varphi_2 - \varphi_1|$<147°, as shown in Fig. 5.5.

The half power beamwidth of the eight-element array with optimum values of $|a_1|$, $|a_2|$, $|b_1|$, and $|b_2|$ is nearly equal to the beamwidth of a uniformly-excited eight-element array, as shown in Fig. 5.6. The difference between the half power beamwidth of the eight-element array and that of a uniformly-excited eight-element array is less than 5 %.

The scan range can then be extended to ±90° by coarse tuning of the inter-element phase differences by increments of 90° (0°, 90°, 180°, and 270°) through the use of quadrature signal generation network along with quadrant and polarity selector switches in each transmitter channel.

5.3 Design of the Wide-Scan Eight-Element Phased Array Operating at K Band

5.3.1 Phased Array Configuration

The block diagram of the wide-scan scalable eight-element phased array operating at K-band is shown in Fig. 5.7. The input signal is divided into two equal single-ended signals using an active divider. Each of these two signals is fed into a four-element scalable subarray. The signals input to the subarrays are converted to differential signals using single-ended to differential signal

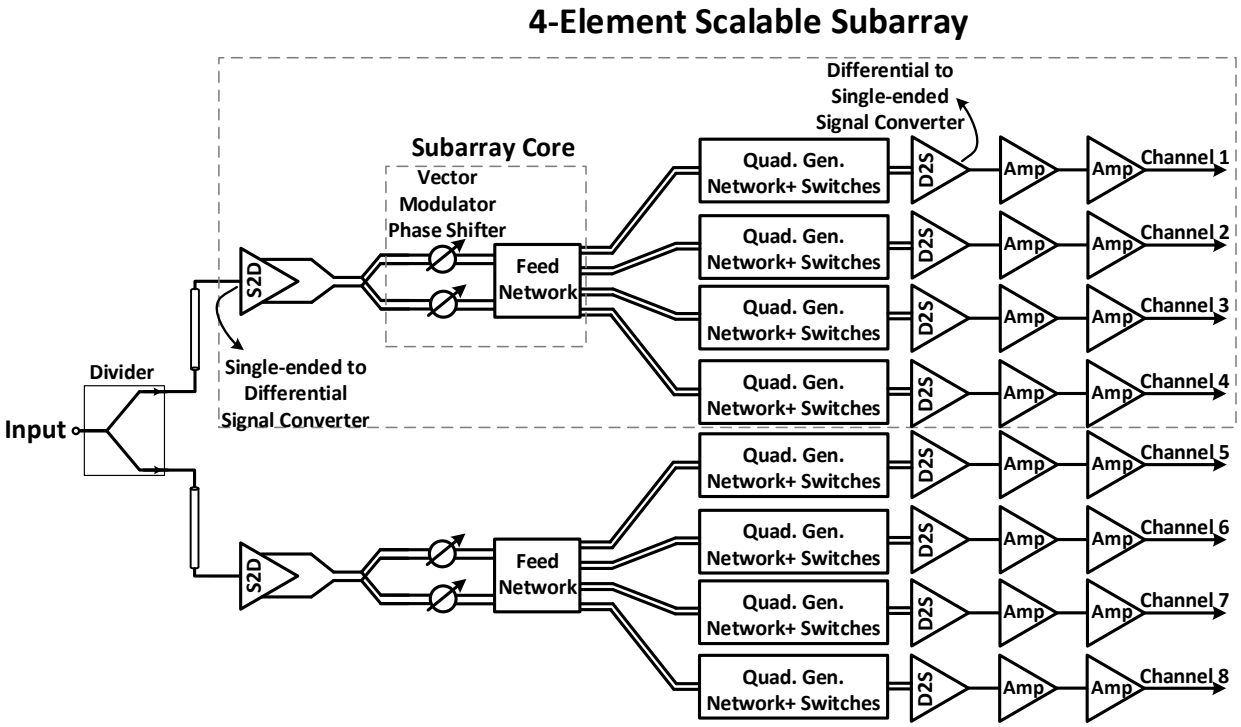


Fig. 5.7. Block diagram of the wide-scan, scalable, eight-element phased array operating at K-band.

converter (S2D), and the differential signals are then fed into the subarray core which includes fully differential vector modulator phase shifters along with the feed network of Fig. 5.2 described in Section 5.2. In the subarray core, the phase shifters' outputs (with a specific relative phase and amplitude) are fed into a feed network which utilizes a vector summation technique to integrate phase-shifting function into the feed (as shown in the block diagram of Fig. 5.2).

The differential signals at the output of the subarray core pass through the quadrature signal generation networks with quadrant selector switches that provide coarse tuning of scan range. The outputs of the quadrature generation networks are then converted back into single-ended signals using active differential to single-ended signal converters (D2S). The single-ended signals at the outputs of the differential to single-ended signal converter blocks pass through two stages of gain and the amplified signals will serve to excite the antenna elements.

5.3.2 Circuit Architecture of the Phased Array

In this sub-section, circuit diagrams and design of the phased array's blocks are presented. Fig. 5.8 shows the circuit diagram of the input active divider which also provides input matching. The input wirebond along with the switched capacitors C_{SW1in} and C_{SW2in}, the inductor L_M, and the transistor M_1 form the input matching network. The wirebond is modeled in HFSS and its S-parameters are used for the design of the input matching network. The switched capacitors are used to allow for tuning the center frequency of the band where input matching is satisfied. In the active divider, the input voltage signal is converted into equal output current signals i_{O1} and i_{O2} using a transconductance stage including the common-source transistor M_1 in conjunction with the cascode transistors M_2, M_3, M_4 and M_5. The current signals i_{O1} and i_{O2} flow through the output inductive loads (denoted by L_P) and generate equal voltage signals, O_1 and O_2, each being fed into one subarray.

An active single-ended to differential signal converter with the circuit diagram of Fig. 5.9 is used as the first stage of each subarray. In this single-ended to differential signal converter, the input signal passes through a common-source stage formed by M_1 to reach node X and is subsequently fed into a common-gate stage (formed by M_3 and M_4) in parallel with a cascode stage (formed by M_2 and M_5), which are non-inverting and inverting ampliers, respectively. Due to the presence of the common-source transistor M_1 at the input of the single-ended to differential signal converter, it presents a relatively high impedance to its preceding stage, thereby not reducing the gain of the preceding stage due to the loading effects. The differential signals v_o^+ and v_o^- at the output of the single-ended to differential signal converter are then fed into the subarray core which includes two vector modulator phase shifters with the circuit diagram of Fig. 5.10 (the same architecture as the phase shifter core presented in Chapter 3) and an active feed network with the

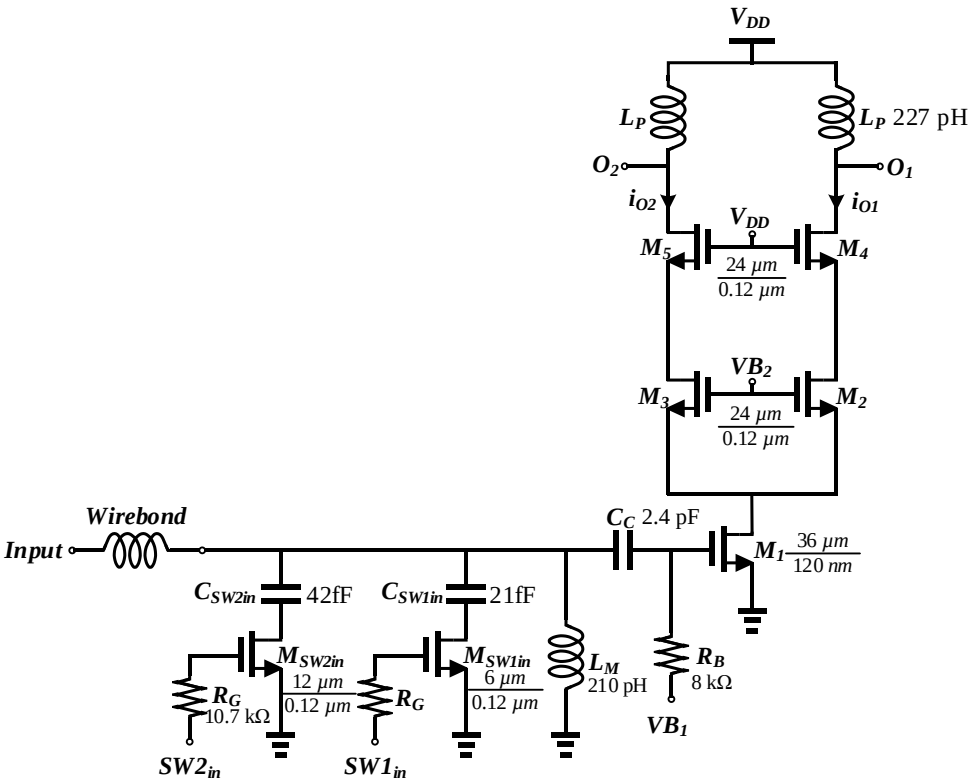


Fig. 5.8. Circuit diagram for the active divider at the input of the phased array.

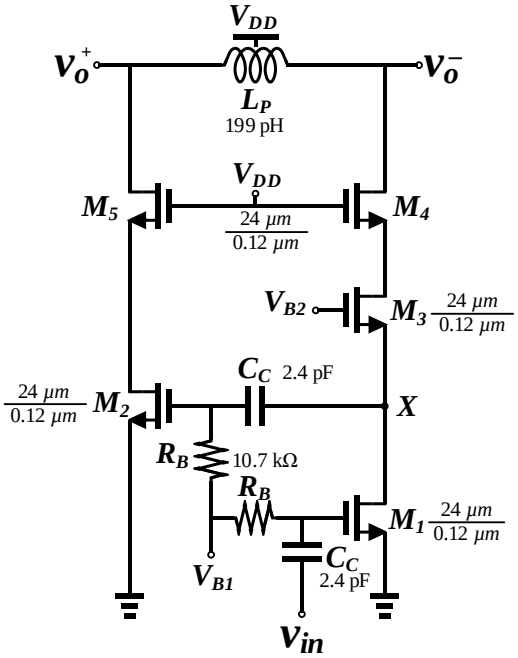


Fig. 5.9. Circuit diagram for the active balun at the input of each subarray.

circuit diagram of Fig. 5.11. The operation principle of the utilized phase shifters, providing 360° of phase tuning with an adjustable output amplitude, is detailed in Chapter 3. The output

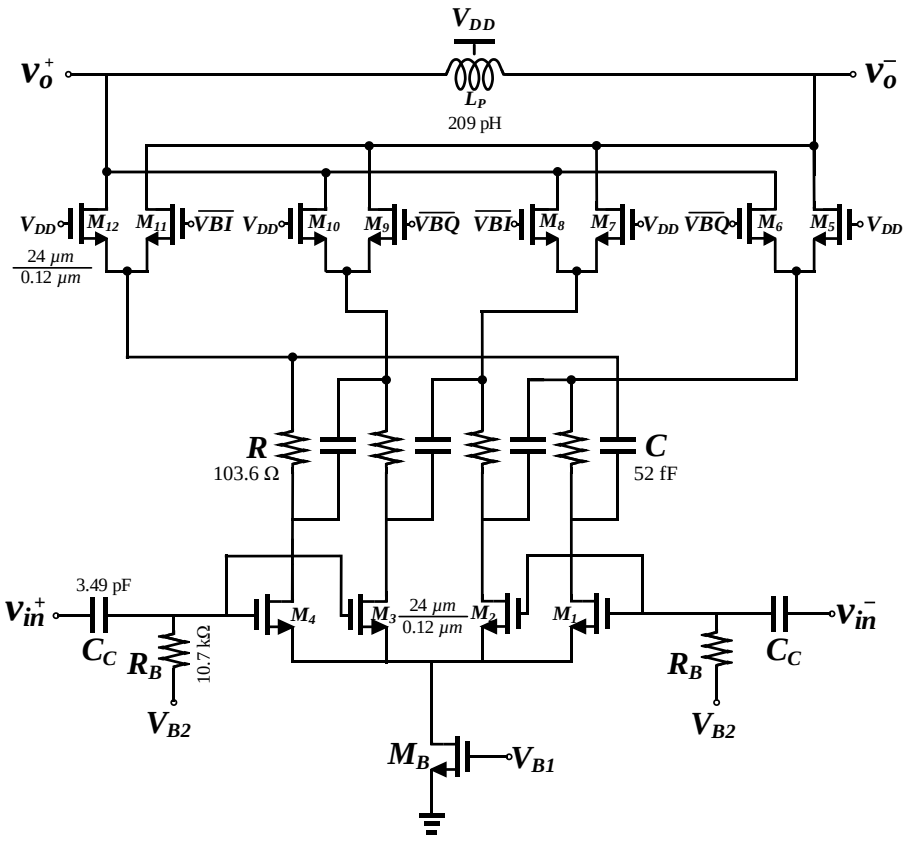


Fig. 5.10. Circuit diagram for the 360° phase shifter with an adjustable output amplitude.

differential signals of the phase shifters are fed into the active feed network which operates based on the described approach in Section 5.2. The feed network has two differential inputs with a relative phase of φ (set by the difference between the insertion phase of the phase shifters) and four differential outputs that are generated by the vector-sum of the two inputs with different weights. As shown in the circuit diagram of Fig. 5.11, each of the two differential inputs are fed into a g_m-cell converting the input differential voltage signals to differential currents. Subsequently, each current signal is unequally divided between four cascode transistors with different sizes (unequal current distribution network). The relative size of the cascode transistors controls the relative weight of their drain-source currents ($i_{e1} - i_{e4}$) which should be equal to the optimum values for $|a|_i$s and $|b_i|$s (i = 1, 2, 3, and 4) in Eqs. (5.1) and (5.2). To satisfy the optimum relative weights for $i_{e1} - i_{e4}$ (equal to 7, 8, 5, and 1, as mentioned earlier), the sizes of the

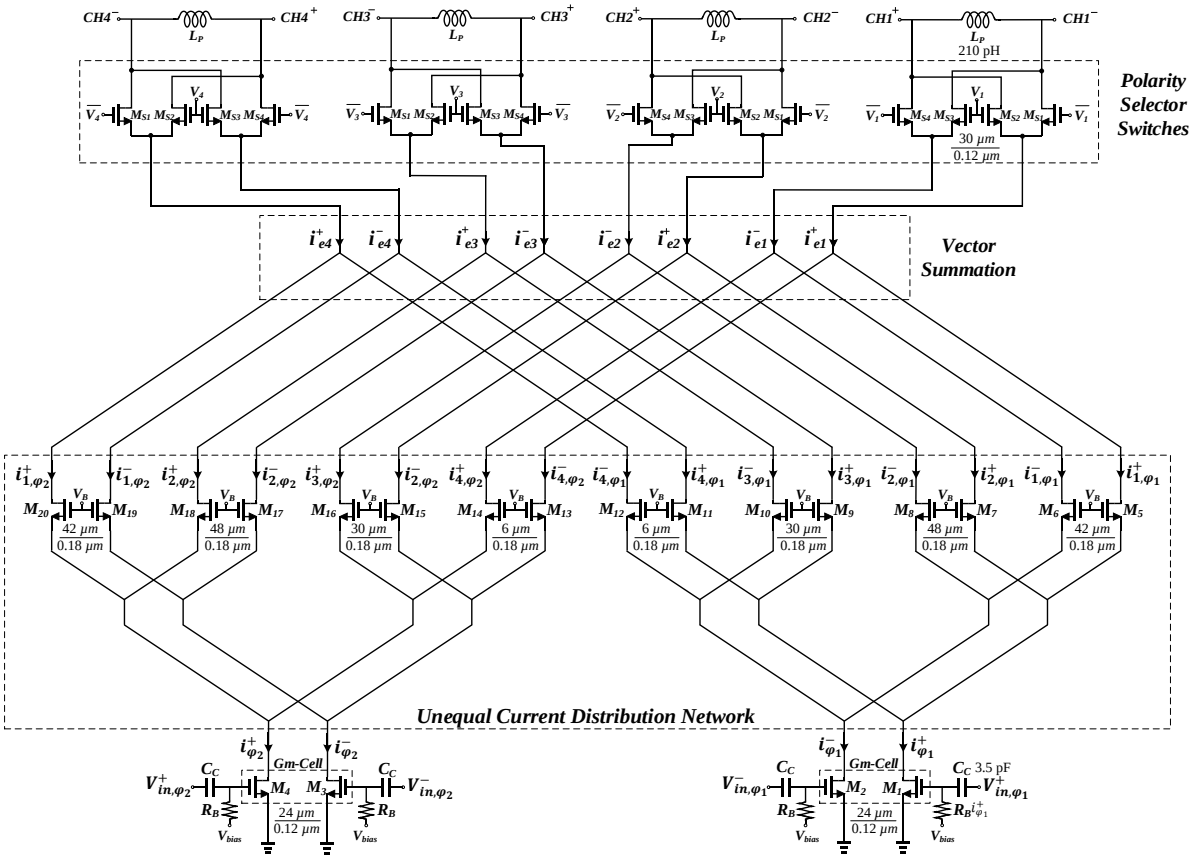


Fig. 5.11. Circuit diagram of the active feed network for the proposed phased array.

transistor pairs ($M_{5,6}$, $M_{19,20}$), ($M_{7,8}$, $M_{17,18}$), ($M_{9,10}$, $M_{15,16}$), and ($M_{11,12}$, $M_{13,14}$) are set to $\frac{42\mu m}{0.18\ \mu m}$, $\frac{48\mu m}{0.18\ \mu m}$, $\frac{30\mu m}{0.18\ \mu m}$, and $\frac{6\mu m}{0.18\ \mu m}$, respectively.

The weighted current signals passing through the current distribution network are then added to generate vector sum signals across the subarray.

To improve matching between the transistors in the current distribution network, their length are set to 0.18 μm, rather than 0.12 μm, and their widths are also set through adjusting the number of fingers for a unit size transistor (here $3\mu m$ width per finger).

The polarities of the vector sum signals $i_{\mathrm{e1}} - i_{\mathrm{e4}}$ are then selected by several switched transistors that are controlled by the complementary signals generated through inverter stages.

Each of the four differential outputs of the feed network (which are also the outputs of the subarray core) are fed into a quadrature generation network with quadrant selector switches, shown

in Fig. 5.12. The quadrature generation network allows for coarse tuning of the excitation phase and inter-element phase differences. In this block, the identical transistors M_1 and M_2 along with a current mode R-C PPF are utilized to generate quadrature currents (i_{Q}^{+}, i_{I}^{+}, i_{Q}^{-}, and i_{I}^{-}). The switched transistors M_3 – M_{10}, controlled by the complementary signals SW_I and SW_Q, are also used to select the quadrant of the differential current signals flowing into the output load. When SW_I is high, the current signals i_{I}^{+} and i_{I}^{-} pass through the output load, and when SW_I is low (SW_Q is high), the current signals i_{Q}^{+} and i_{Q}^{-} pass through the outptus. The quadrant selector switches in Fig. 5.12 along with the polarity selector switches in Fig. 5.11 allow for coarse tuning of the inter-element phase differences by 0°, 90°, 180°, and 270°. The differential outputs of the quadrature generation network are fed into a differential to single-ended signal converter with the circuit diagram of Fig. 5.13. In the proposed differential to single-ended signal converter, the input signals v_{in}^{+} and v_{in}^{-} pass through a common-source stage to reach the nodes X and Y, respectively. In order to generate similar response from v_{in}^{+} to the node X and v_{in}^{-} to the node Y, a diode-connected configuration is used for M_5. The signals at the nodes X and Y pass though a cascode stage (formed by M_6 and M_7) and a common-gate stage (formed by M_2 and M_3), respectively, to reach the output. Therefore, the differential to single-ended signal converter inverts and amplifies v_{in}^{-}, however, v_{in}^{+} is amplified but not inverted by the converter. In the described circuit, a common-source stage is selected for the input so that the differential to single-ended signal converter can have a high input impedance thereby not reducing the gain of its preceding stage due to the loading effects. The single-ended output of the differential to single-ended signal converter is fed into two stages of amplifiers shown in Fig. 5.14 to generate the antenna's excitation signal. The amplifiers in Fig. 5.14 have a cascode configuration and provide an overall gain of approximately 11.5 dB at 24 GHz. The second stage of amplifier includes an output matching network comprising of the output

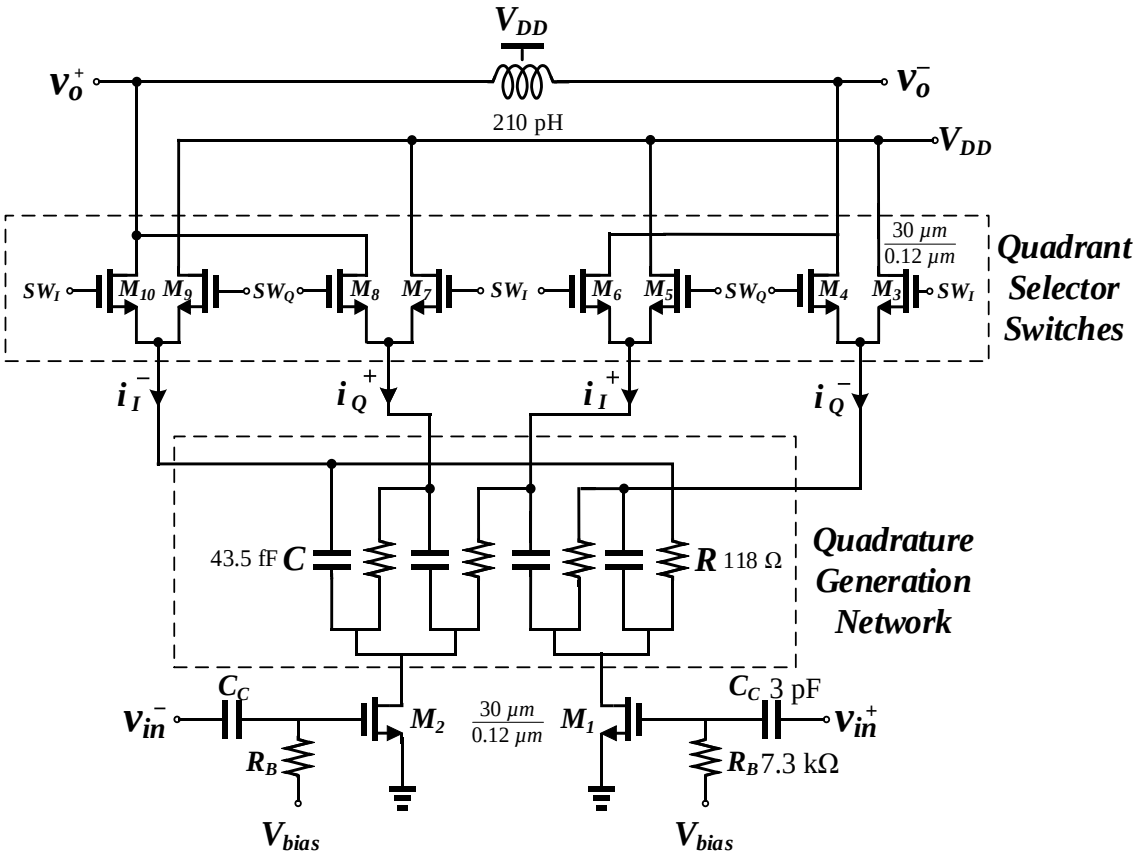


Fig. 5.12. Circuit diagram for the quadrature generation network with quadrant selector switches.

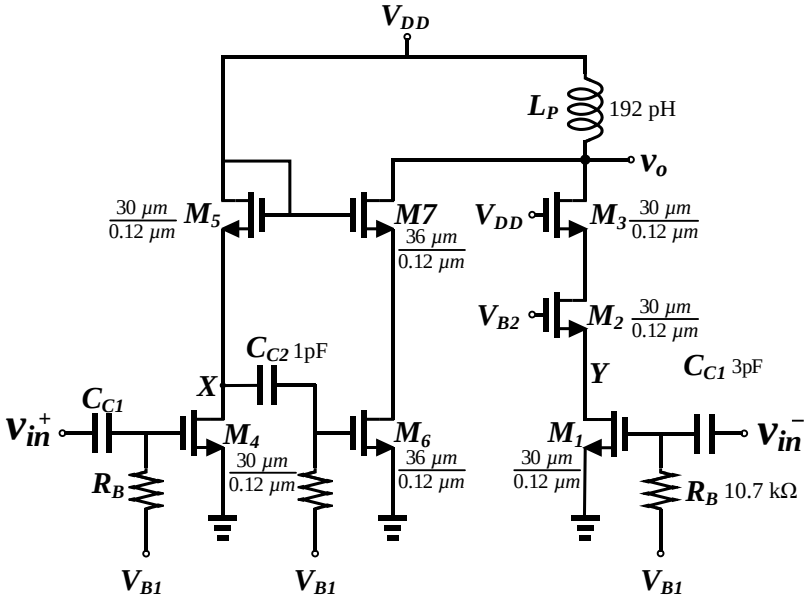


Fig. 5.13. Circuit diagram for the proposed differential to single-ended signal converter.

wirebond model, switched capacitors C_{SW1} and C_{SW2}, the inductor L_P, and the transistor M_2. The output wirebond is modeled in HFSS and its S-parameters are used for design of the output

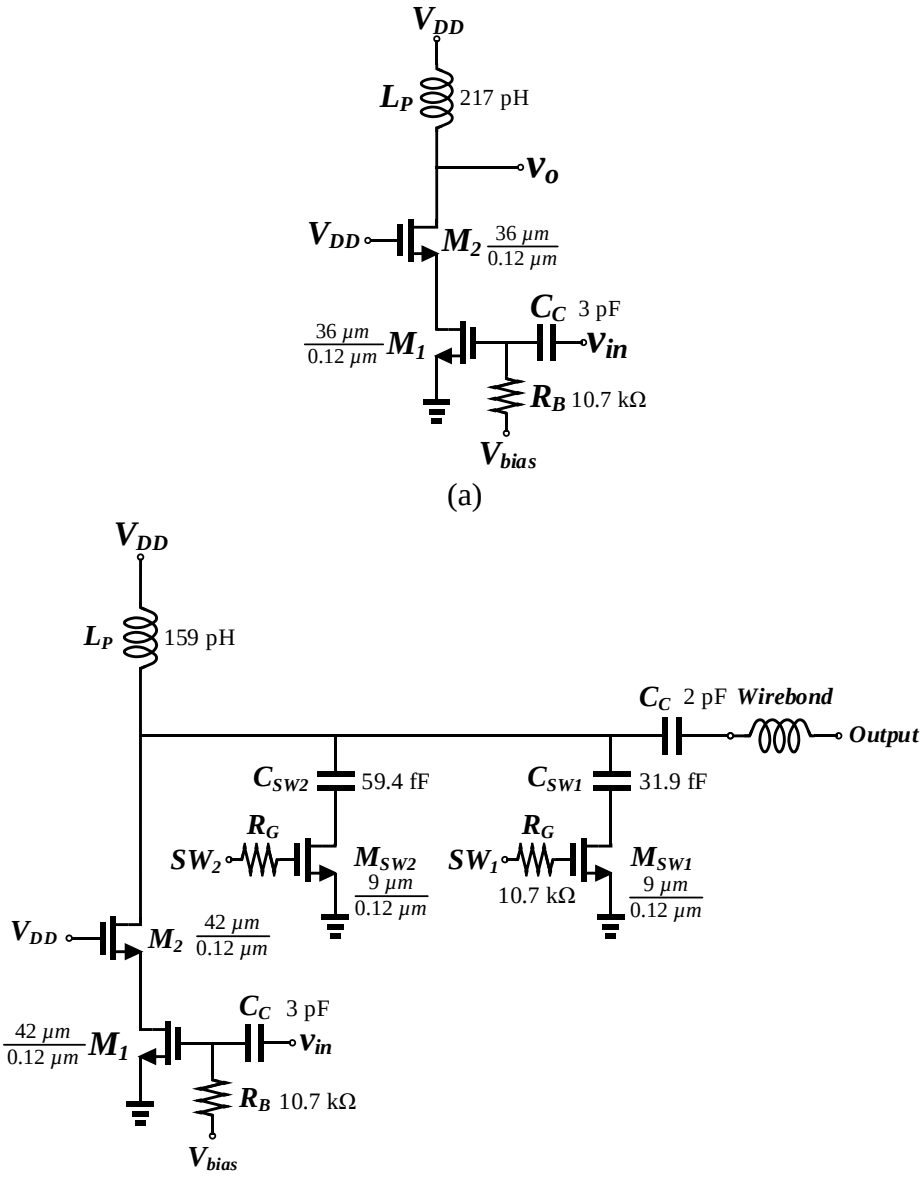


Fig. 5.14. Circuit diagrams for (a) the first stage and (b) the second stage amplifier at the output of each channel.

matching network. The switched capacitors C_{SW1} and C_{SW2} are used to allow for tuning the center frequency of the output matching network.

It should be noted that in this phased array, each subarray employs two vector modulator phase shifters that provide 360º of phase tuning with an adjustable output amplitude. Gain tunability of the utilized phase shifters allows for maintainig the maximum value of array factor as the scan range is tuned. It also allows for a better control over the excitation phases and amplitudes in order

to generate a desired array factor even with the presence of errors which can be due to different reasons such as device mismatch, variations of process, voltage, and temperature, limited accuracy of EM modeling, and PCB fabrication errors.

5.4 Simulation and Measurement Results

The simulated insertion phase, gain, input and output reflection coefficient of the eight-element phased array versus frequency as well as the normalized array factor at 24 GHz at the scan angles of 0°, ±5°, ±10°, and ±15° are shown in Figs. 5.15–5.21. Array factor is calculated using a MATLAB code which utilizes the simulated S-parameters. The distribution of the signal phase and amplitude across the desinged array synthesizes array factors satisfying the specified criteria on the sidelobelevels and half power beamwidth. The array factors shown in Figs. 5.15–5.21 (providing ±15° of scan range) are obtained by adjusting only eight analog signals that are used to control the insertion phase and gain of four vector modulator phase shifters in the feed network.

According to Figs. 5.15–5.21, the input and output reflection coefficients are smaller than -10 dB within 23-24.5 GHz. Due to the multiple switched capacitors employed in the matching networks, the center frequency of the input and output matching networks can be tuned, as shown in Fig. 5.22.

The simulation results showing the normalized array factor at different scan angles within ±90° are provided in Fig. 5.23. The scan angles below -15° and above 15° are obained by adjusting the states of the polarity and quadrant selector switches in conjunction with tuning the eight analog controls.

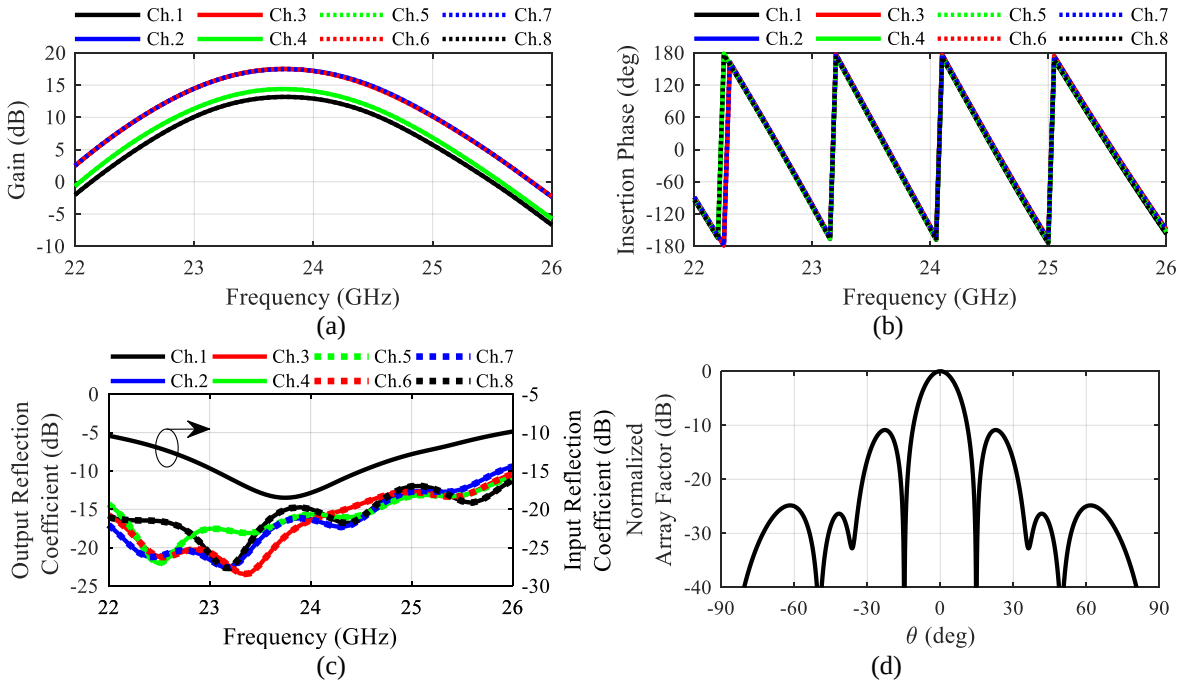


Fig. 5.15. Simulated frequency response of the eight-element phased array at the scan angle of 0° (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.

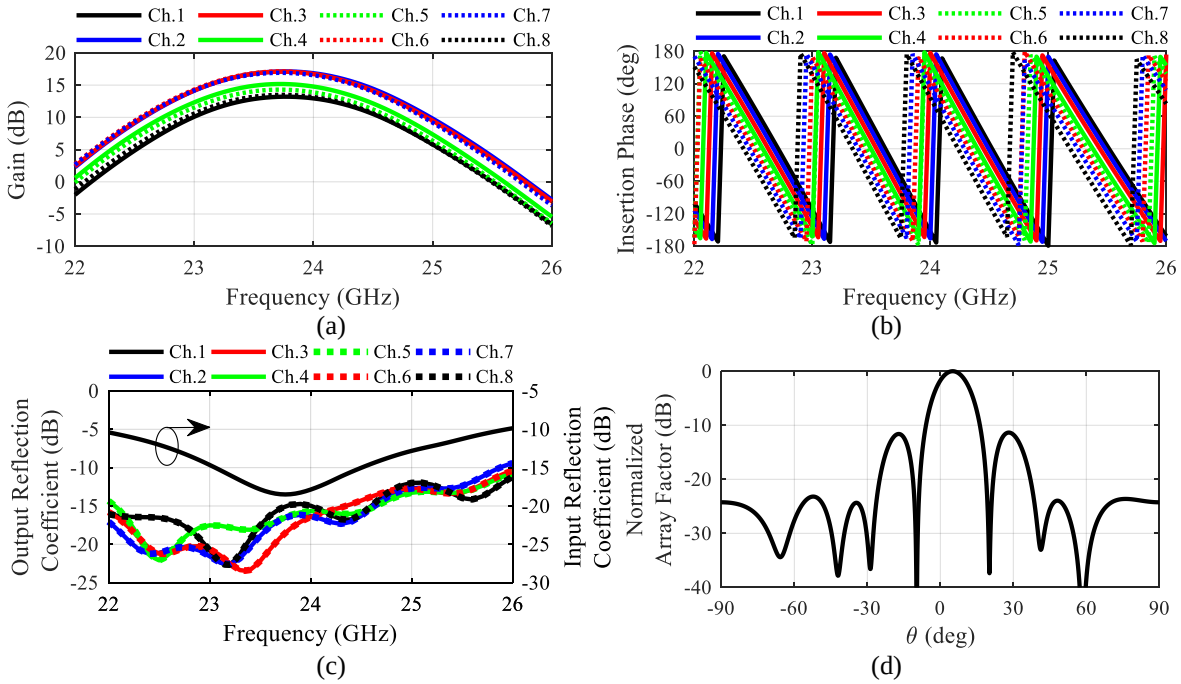


Fig. 5.16. Simulated frequency response of the eight-element phased array at the scan angle of 5°. (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.

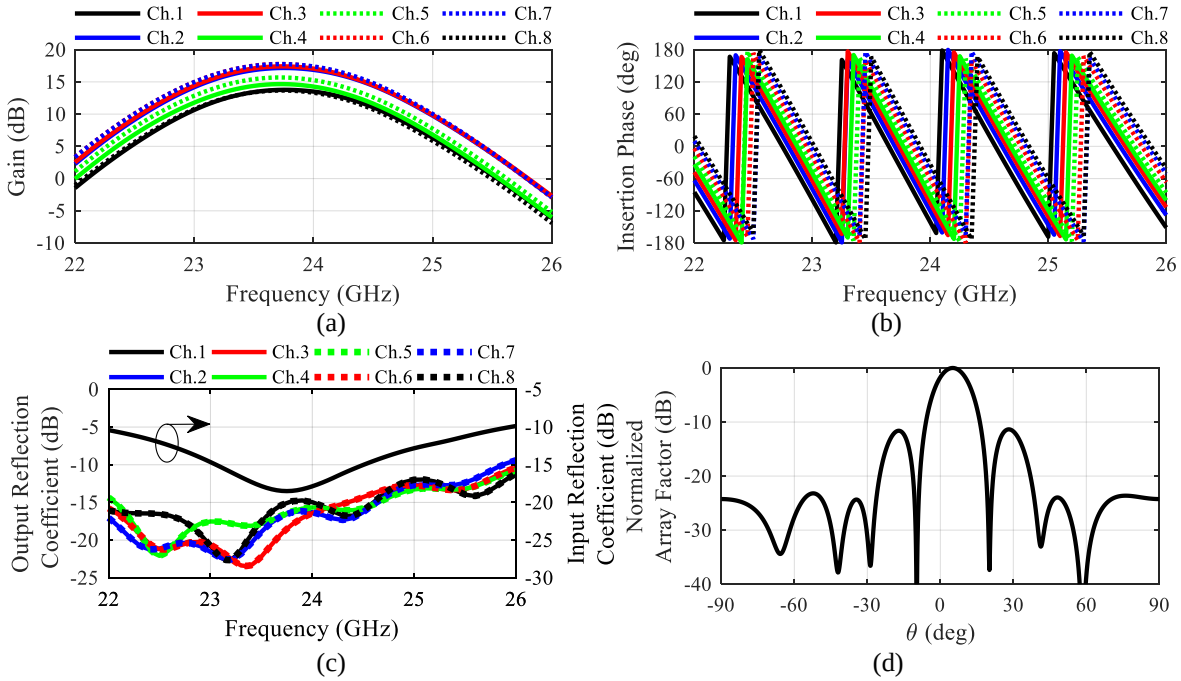


Fig. 5.17. Simulated frequency response of the eight-element phased array at the scan angle of -5°. (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.

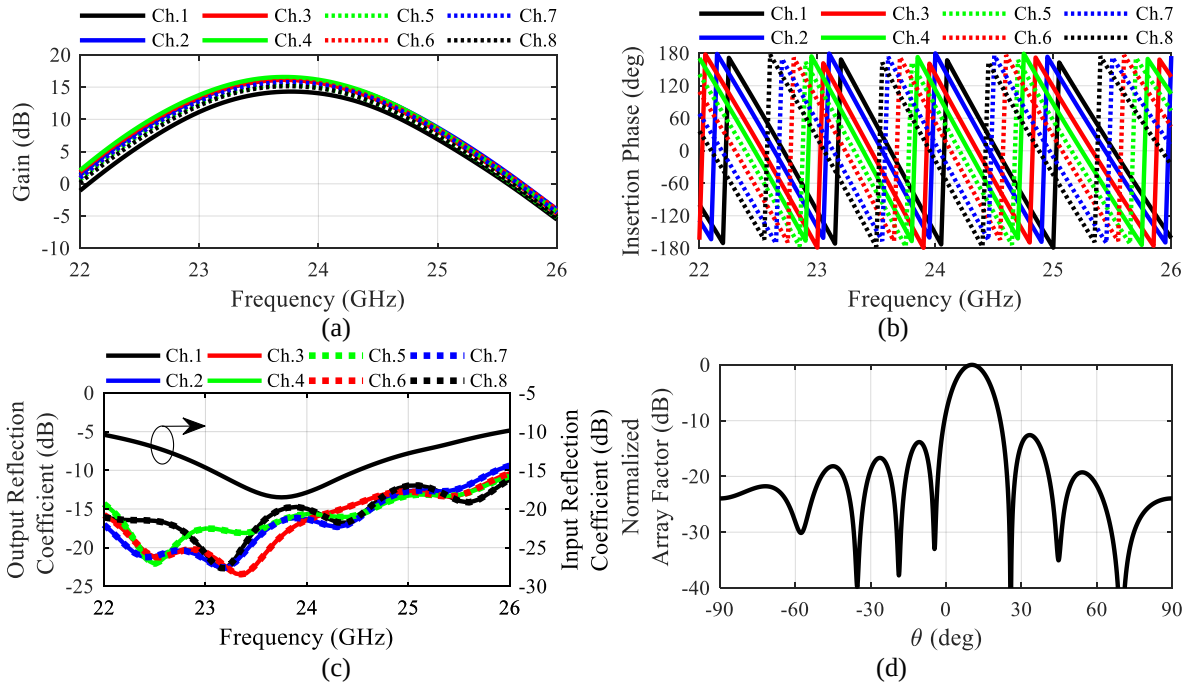


Fig. 5.18. Simulated frequency response of the eight-element phased array at the scan angle of 10°. (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.

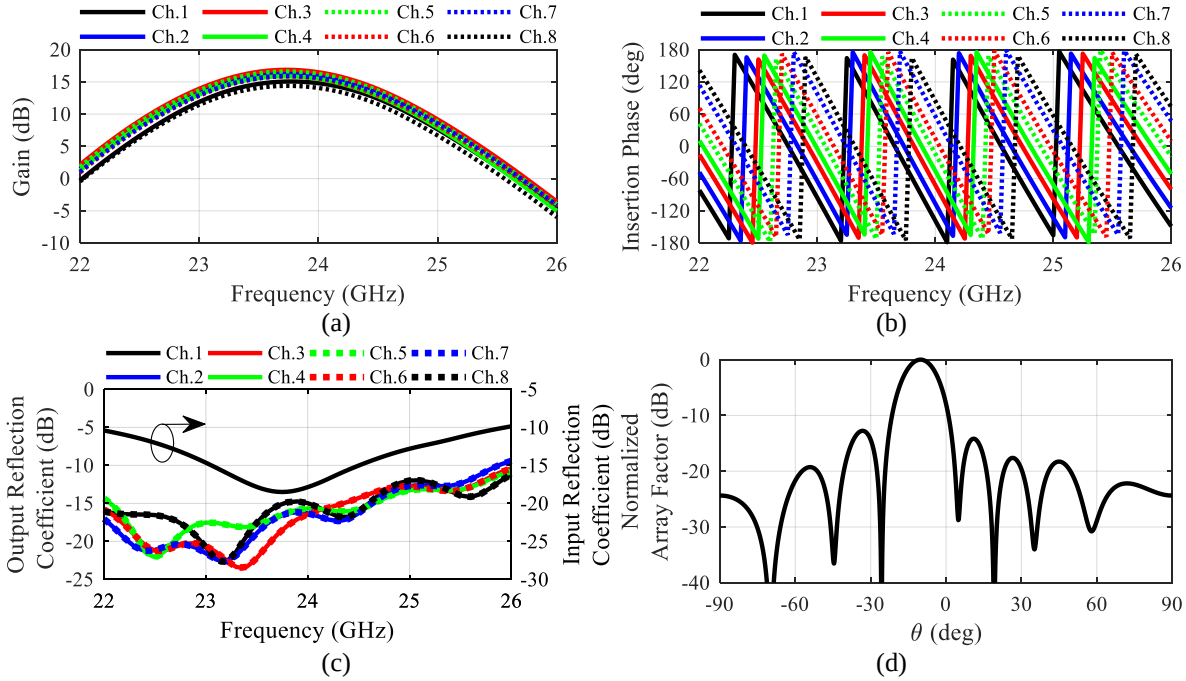


Fig. 5.19. Simulated frequency response of the eight-element phased array at the scan angle of -10°. (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.

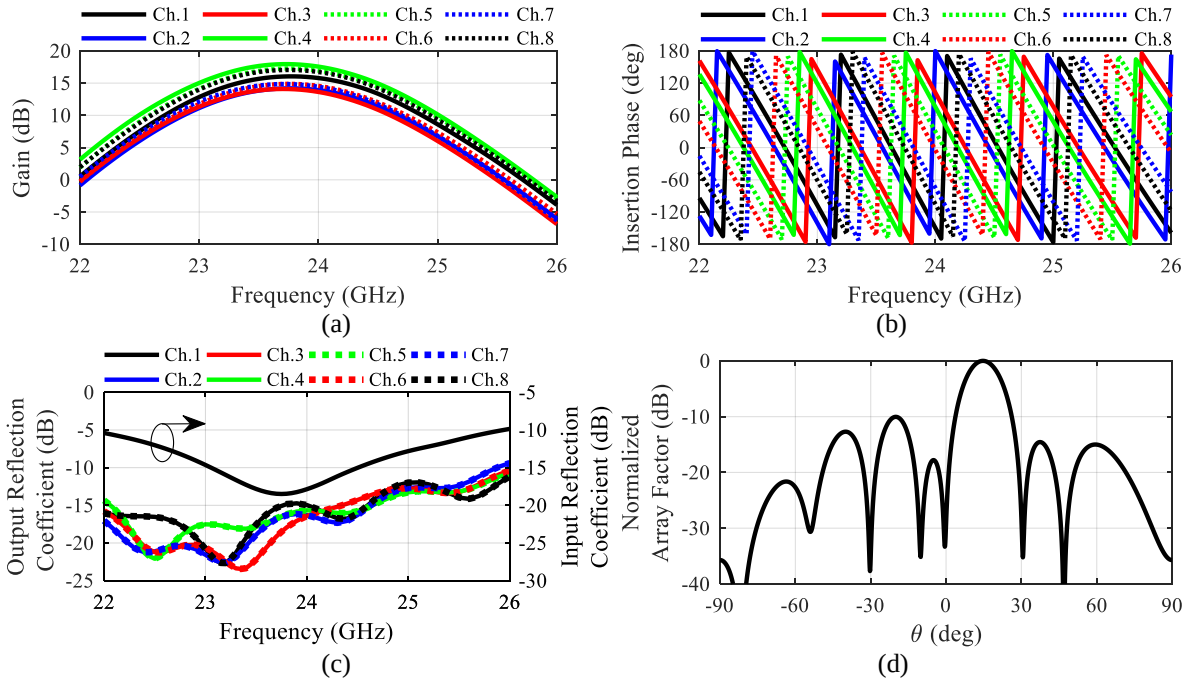


Fig. 5.20. Simulated frequency response of the eight-element phased array at the scan angle of 15°. (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.

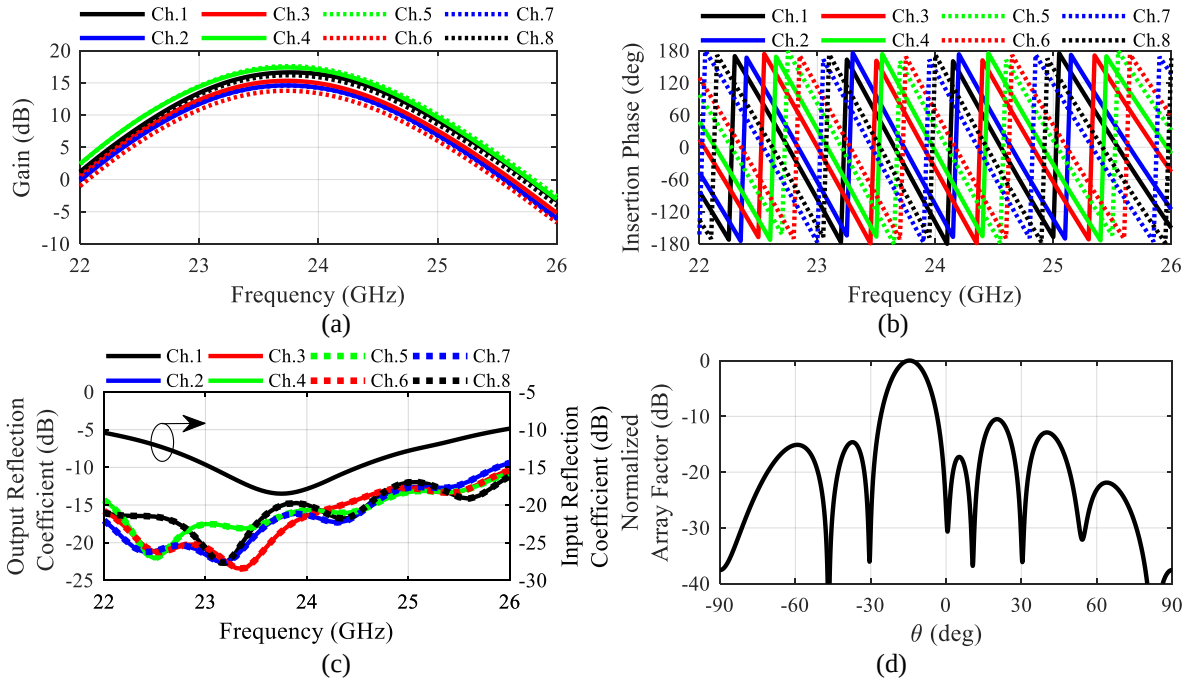
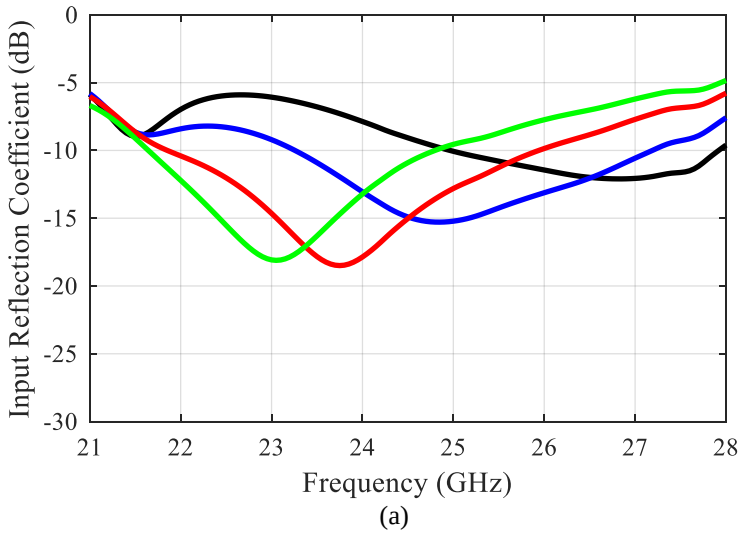
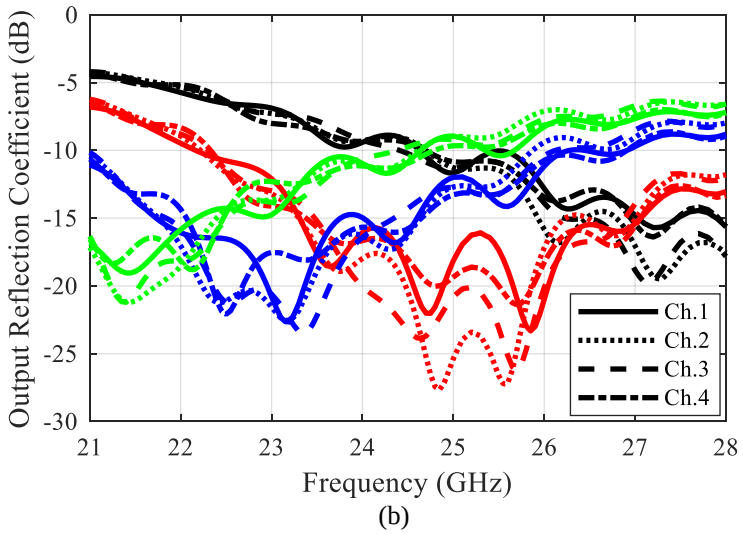


Fig. 5.21. Simulated frequency response of the eight-element phased array at the scan angle of -15°. (a) Gain and (b) Insertion phase versus frequency for different channels within the array. (c) Input reflection coefficient and output reflection coefficient of the phased array versus frequency at different channels within the array. (d) Normalized array factor at 24 GHz.



(a)



(b)

Fig. 5.22. (a) Simulated input reflection coefficient versus frequency for different switching states of (SW_{2in}, SW_{1in}). Green lines: (SW_{2in}, SW_{1in}) = (1, 1), blue lines: (SW_{2in}, SW_{1in}) = (1, 0), red lines: (SW_{2in}, SW_{1in}) = (0, 1), and black lines: (SW_{2in}, SW_{1in}) = (0, 0). (b) Simulated output reflection coefficient versus frequency for different switching states of (SW_2, SW_1). Green lines: (SW_2, SW_1) = (1, 1), blue lines: (SW_2, SW_1) = (1, 0), red lines: (SW_2, SW_1) = (0, 1), and black lines: (SW_2, SW_1) = (0, 0).

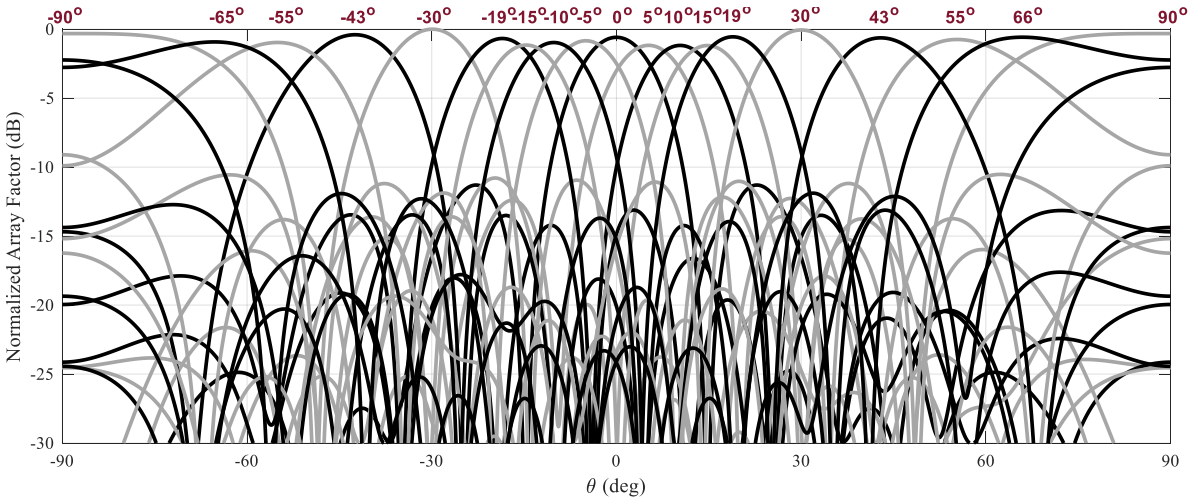


Fig. 5.23. Simulated normalized array factor for the eight-element phased array at different scan angles at 24 GHz.

Die photo of the fabricated 130-nm CMOS eight-element phased array with a total die size of 1.68 mm × 3.954 mm is shown in Fig. 5.24. To measure the chip performance, it is is mounted on a four-layer PCB comprising of a 10 mil Rogers RO3006 dielectric on top of a 4 mil prepreg connected to a 16 mil FR4 substrate. All RF and dc pads are wirebonded to PCB. The input and output GSG pads are wirebonded to 50 Ω grounded coplanar waveguide lines on the top layer of the PCB, and the 50 Ω lines are connected to amphenol high frequency SMA end launch connectors. The performance of the phased array, shown in Fig. 5.25, is characterized using an Agilent E8364C PNA network analyzer. The wirebonds connecting the input and outputs of the array to 50 Ω lines are modeled using ANSYS HFSS electromagnetic simulator, and their scattering parameters are accounted for in the design of the RF input and output matching networks (all the RF ports are matched to 50 Ohm).

To measure the beam steering performance of the phased array, the control voltage of the phase shifters are initially set to the original values used in the circuit simulation. The S-parameters are measured between the input port and each of the output ports while the adjacent output ports are terminated with 50 Ω loads. Using the measured S-parameters, the array factor is calculated using

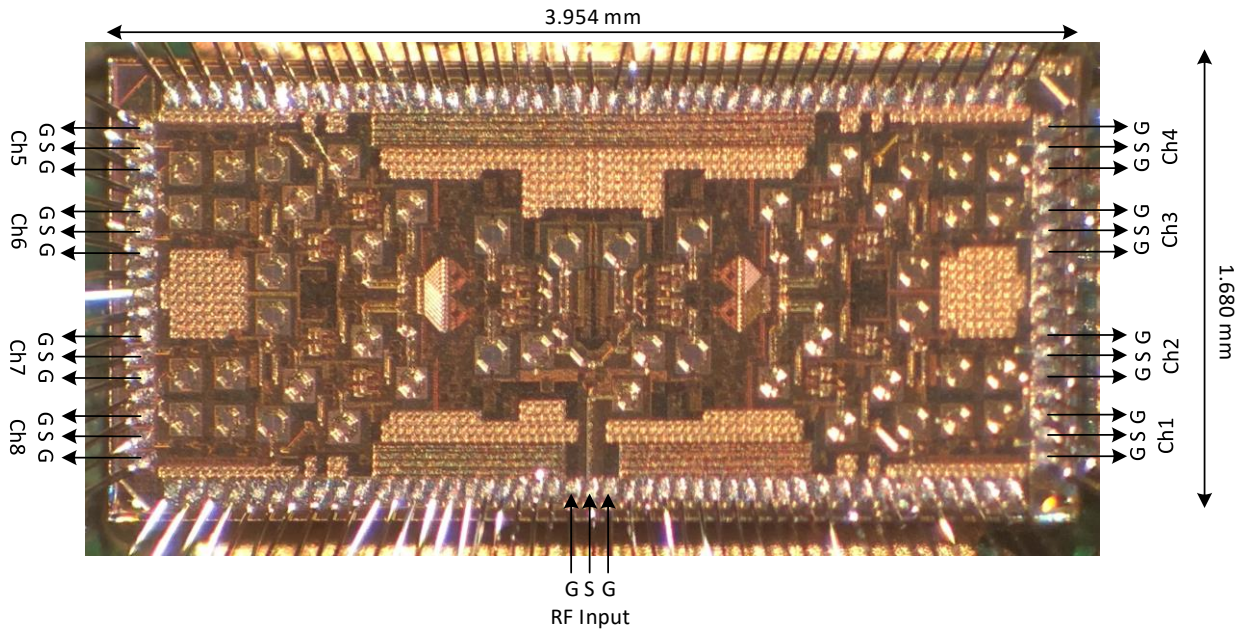


Fig. 5.24. Die photo of the fabricated eight-element phased array (die size = 1.68 mm × 3.954 mm).

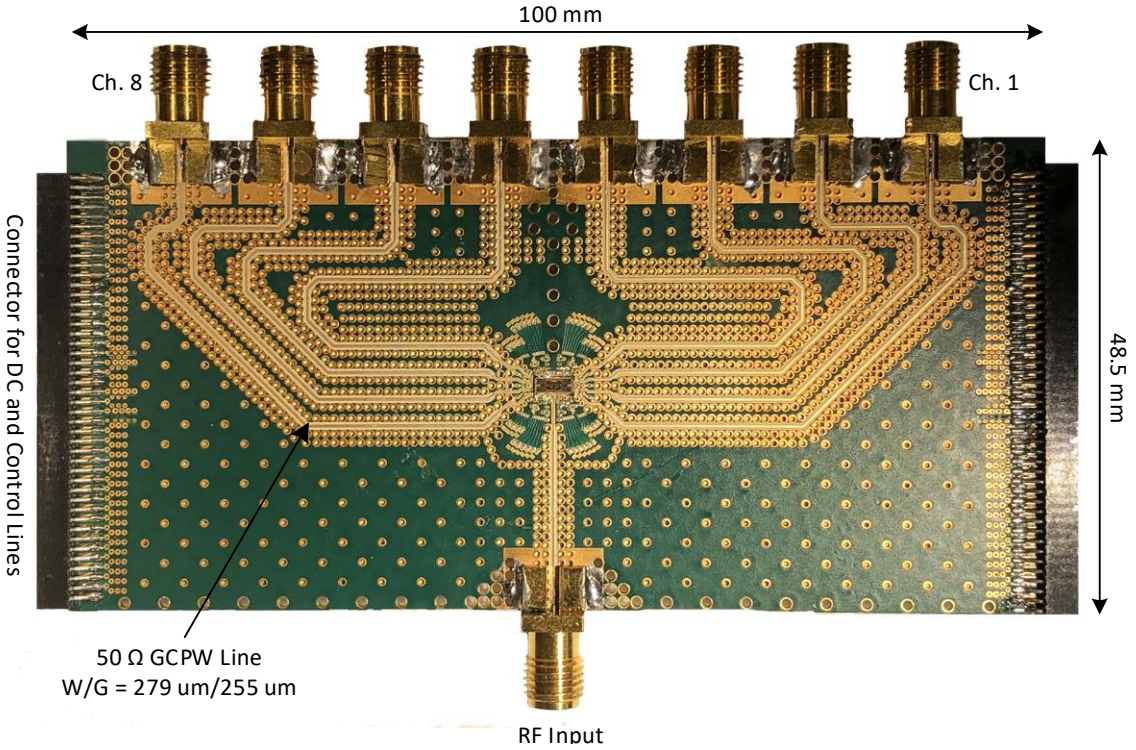


Fig. 5.25. Top view of the 8-element CMOS phased array chip bonded on a four-layer PCB.

a MATLAB code. Fig. 5.26 shows the measured frequency response of the four channels within one subarray when the phase shifters' control voltages are set to the values corresponding to the

scan angle of 0° in circuit simulations. It should be noted that to improve the input and output matching in measurements, the switching states of (SW_{2in}, SW_{1in}) and (SW_{2in}, SW_{1in}) are both set to (0,1), while in the simulations, they were both set to (1,0).

According to Fig. 5.26, the center frequency of the channels 1 and 2, as well as the channels 3 and 4 are offset by approximately 200 MHz, which is primarily due to the slight difference in the layout and wirebond connections of the channels. The phases of the channels 1 (or 4) and 2 (or 3) are also different by approximately 105° within the band 23-24 GHz, which is mainly due to the difference in the center frequency of the channels (in fact, the phase of each channel varies by approximately 95° within 200 MHz).

To cancel the phase difference between the subarray's channels at the scan angle of 0°, two pieces of transmission lines with electrical lengths of 116° and 98° at 24 GHz are added to channels 2 and 3, respectively. As a result, the entire channels can be in phase at 24 GHz to provide the scan angle of 0°. The corrected insertion phase at different channels of the subarray and the resulting array factor at the scan angle of 0° are also shown in Fig. 5.26. After applying this correction, the control voltages are fine-tuned around the values set in the circuit simulations to steer the beam to other scan angles. The measured array factor for the eight-element phased array which is controlled by eight analog signals and sixteen switches are shown in Fig. 5.27. The presented phased array provides ± 90° of scan range at 24 GHz with smaller than -9 dB of sidelobe levels and less than 2 dB of variation in maximum array factor over the entire scan range.

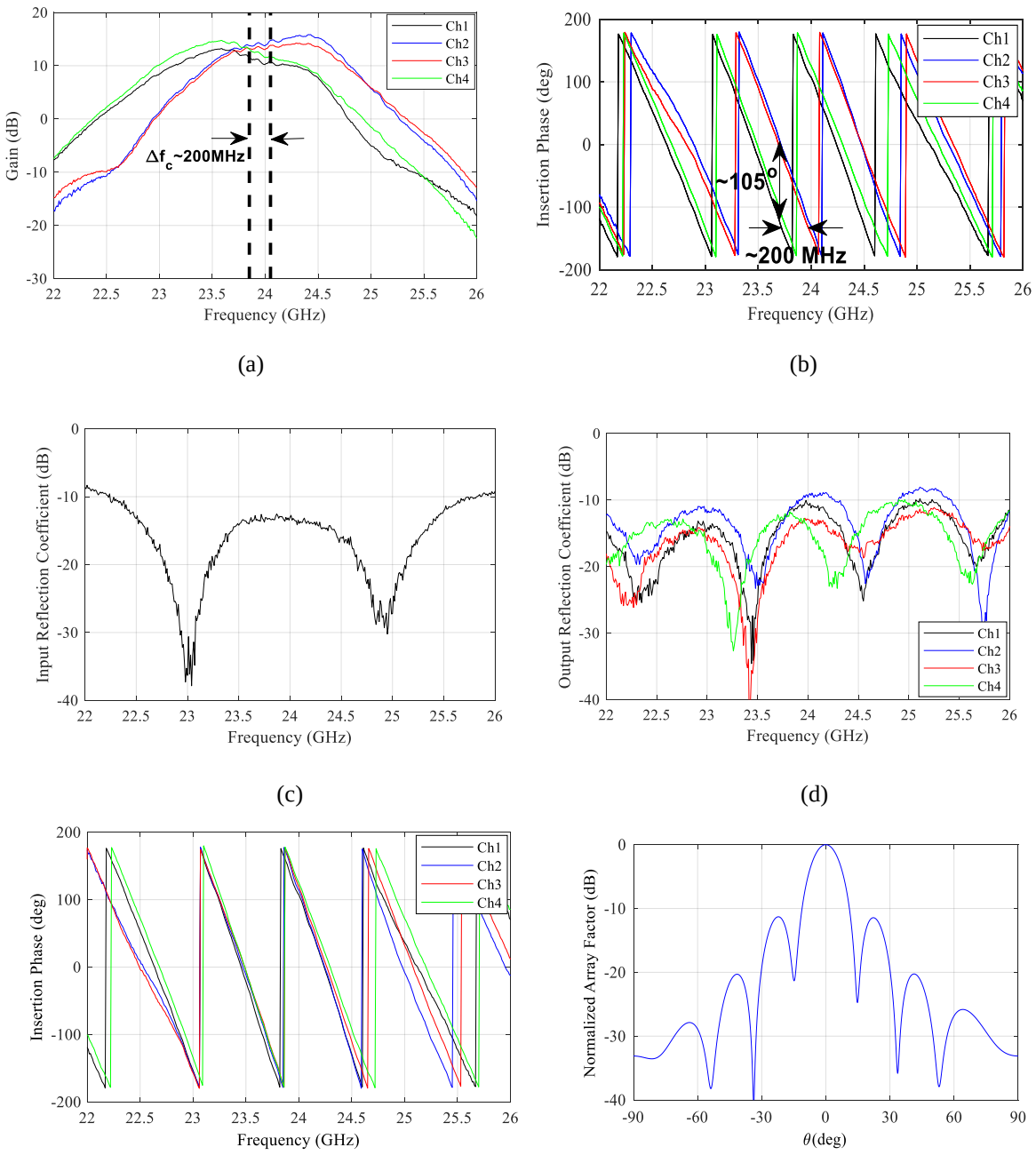


Fig. 5.26. Measured frequency response of each channel within a subarray when the phase shifters' control voltages are set to the values corresponding to the scan angle of 0° in circuit simulations. (a) Gain for different channels of one subarray. (b) Insertion phase for different channels of one subarray. (c) Input reflection coefficient and (d) output reflection coefficient at different channels of one subarray. (e) Insertion phase for different channels of one subarray after adding two pieces of transmission lines with electrical lengths of 116° and 98° at 24 GHz to channels 2 and 3, respectively. (f) Normalized array factor at the scan angle of 0°.

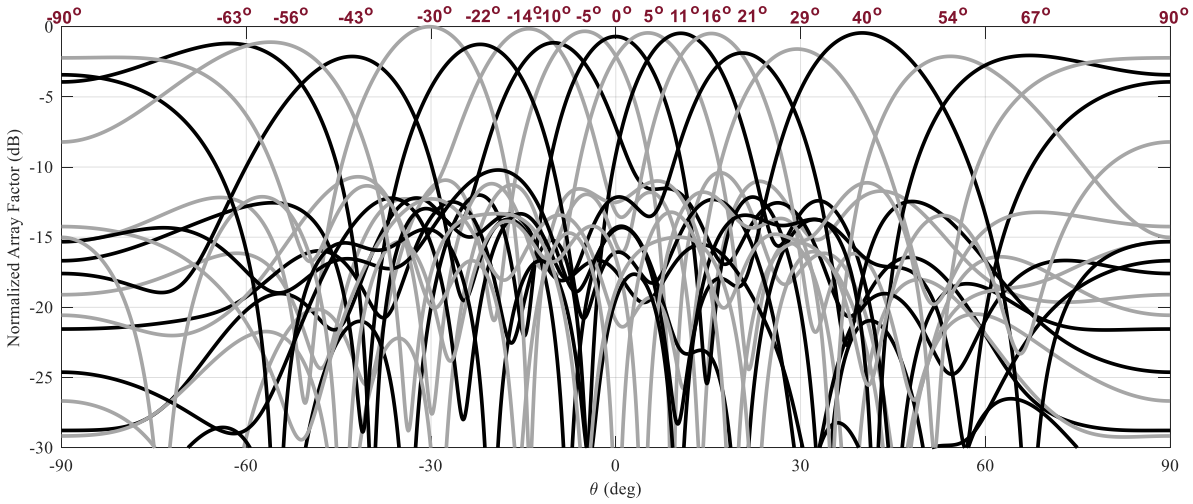


Fig. 5.27. Measured normalized array factor for the eight-element phased array at different scan angles at 24 GHz.

5.5 Conclusion

A new architecture for scalable phased arrays with reduced number of phase shifters has been presented. In this phased array architecture, a vector summation technique is used to integrate the phase shifting function into the array's feed network in order to reduce the required number of phase shifters thereby, reducing the array's complexity. As a proof of principle, a wide-scan eight-element phased array employing four phase shifters has been designed and fabricated in 130-nm CMOS process at K-band. The phased array, controlled by eight analog signals and sixteen switches, provides ±90^{o} of scan range with sidelobe levels smaller than -9 dB and a half power beamwidth close to the beamwidth of an eight-element uniform array. The chip occupies an area of 6.64 mm^2 and consumes 682 mW of dc power.

Chapter 6: Conclusion and Recommendations for Future Work

6.1 Thesis Summary

Phase shifters are one of the key components of phased arrays and are responsible to adjust the signal phase across the array elements. In general, phase shifters along with their control circuitry play a major role in determining the complexity and size of conventional phased arrays. In this thesis, to reduce phased arrays' complexity and size without degrading their performance, two new architectures and design techniques for scalable phased arrays with significantly reduced number of phase shifters and control signals are presented. Two new integrated phase shifters with small size, simple control, and low power consumption are also presented for further reduction of phased arrays' complexity and size.

The phase shifters are presented in Chapters 2 and 3 followed by detailed analysis of the low-complexity phased array architectures in Chapters 4 and 5.

In Chapter 2, a new vector sum phase shifter operating based on the summation of rotating orthogonal vectors is presented. In this phase shifter, the phases of the orthogonal vectors I and Q are varied (while maintaining the relative phase between I and Q) in conjunction with their amplitude ratio, all by tuning only one control parameter, to vary the vector sum phase while limiting its magnitude variation. Since the equal phase variation (rotation) of I and Q vectors control the phase of the vector sum signal while preserving its magnitude, this phase shifter allows for varying the vector sum phase with minimum magnitude variation over the phase tuning range. The circuit architecture and detailed analyses of the proposed phase shifter in addition to an

optimum design for maximizing the phase tuning range with a constant output amplitude have been presented. A fully differential CMOS phase shifter operating based on the summation of rotating I and Q vectors is designed at K band and the simulated performance of the phase shifter is shown. In the phase shifter's circuit topology, all the tasks of vector (I and Q) generation, vectors' amplitude and phase variation, and vector summation are performed in a single stage to save both power and area. To increase the phase tuning range, multiple switched varactors are employed in this phase shifter. Subsequently, it is connected to an active balun at the input and a buffer at the output that also provide input and output matching to allow for the phase shifter operation as a stand-alone IC. The circuit, fabricated in 130-nm CMOS process provides 300° of continuous phase tuning at K-band with a total power consumption of 18.5 mW, while occupying a chip area of 0.434 mm^2 (excluding the pads). The phase shifter core consumes only 7.8 mW, and its corresponding area is 0.045 mm^2. This phase shifter provides continuous phase tuning while consuming a relatively low dc power and occupying a small chip area, which makes it a potential candidate for integrated phased arrays in automotive radars and 5G mobile terminals.

In Chapter 3, a CMOS vector modulator phase shifter operating at K and KA bands has been presented. The center frequency of operation can be tuned within 26−28 GHz while the phase shifter's instantaneous 3-dB bandwidth is 3 GHz. In the circuit topology of this phase shifter, all the tasks of vector generation, gain control, and vector summation are performed in a single stage (which is called phase shifter core) to save chip area and power consumption. The phase shifter core provides 360° of continuous phase tuning and an adjustable amplitude for the output signal while occupying only 0.063 mm^2 of chip area and consuming 7.8 mW of power.

The phase shifter core is connected to active baluns that also serve as the matching networks at the input and output to form a single-ended input single-ended output stand-alone IC. The chip

has been designed and fabricated in 130-nm CMOS process. It consumes 27 mW of power over the entire phase tuning range an occupies 0.284 mm^2 of area (excluding the pads). The phase shifter exhibits a negligible gain variation over the phase tuning range and a decent phase stability with respect to the input power level. Considering the phase and gain tunability, small size, bandwidth, and frequency tunable range of the phase shifter described in Chapter 3, it is a suitable candidate for integrated phased arrays in automotive radars as well as 5G applications.

In Chapters 4 and 5, two new phased array architectures with significantly reduced number of phase shifters and control signals are presented. In these phased arrays, phase shifting function is integrated into the feed network of a subarray through vector summation in order to reduce the number of phase shifters. A number of subarrays can be connected to form a larger array providing a narrow beamwidth.

In the phased array presented in Chapter 4, a new RF feed network incorporating vector summation is used to allow for the control of signal phase and amplitude along an N-element subarray by a single phase shifter and N number of variable gain amplifiers. This phased array has a limited scan range since the signals across the array elements are all derived from a single phase shifter. Increasing the number of elements (N) in one subarray employing a single phase shifter reduces the scan range. To maintain the scan range while increasing the number of array elements, multiple subarrays can be connected.

A design technique based on particle swarm optimization algorithm has also been presented for maximizing the scan range of the N-element subarray employing a single phase shifter while limiting the sidelobe levels and half power beamwidth. As a proof of concept, an eight-element transmit phased array comprising of two four-element subarrays is designed and fabricated at the Ku-band. The fabricated phased array provides a large scan range and a small ratio of the number

of phase shifters to the number of array elements compared to other phased arrays with reduced number of phase shifters. This phased array is a potential candidate for long-range automotive radars requiring a limited scan range.

In Chapter 5, a new wide-scan, integrated, scalable phased array with a reduced number of phase shifters and simple control is presented. In this phased array, where phase shifting function is integrated into the feed network of a scalable subarray through incorporating vector summation in the feed network, the total number of phase shifters and their corresponding control signals are reduced by a factor of two as compared to conventional phased arrays.

An eight-element phased array including two four-element subarrays is designed using an optimization algorithm (based on particle swarm optimization) to provide ±90° of continuous scan range with better than -10 dB of sidelobe levels. Each subarray employs two phase shifters with adjustable output amplitude (the phase shifters are designed based on the phase shifter core presented in Chapter 3) and is designed to provide ±15° of continuous scan range, corresponding to an average inter-element phase difference of ±45°. A quadrature signal generation network along with quadrant selector switches are also utilized at each channel to allow for increasing the inter-element phase differences up to ±180° and providing a scan range of ±90°.

The eight-element phased array is designed and fabricated in 130-nm CMOS process. The integrated phased array provides a wide scan range while consuming 690 mW of dc power and occupying 6.636 mm^2 of chip area. This phased array is a promising candidate for applications in 5G communications and automotive radars for ADAS and autonomous vehicles.

In conclusion, this thesis has presented several approaches to design low-complexity scalable phased arrays with the goal of facilitating their widespread use in low-cost communication and radar applications.

6.2 Future Work

This thesis has presented low-complexity phased array architectures that are applicable for the design of receive as well as transmit phased arrays. In this work, two phased array transmitters operating at Ku and K bands have been designed and fabricated. One can also design low-complexity phased arrays operating in receive mode. Furthermore, considering that in the described architectures, a transmit phased array can be converted into a receive phased array by reversing the signal flow direction and interchanging the dividers and combiners, it is possible to design low-complexity phased array transceivers based on the proposed architectures.

For the design of receive phased arrays, the noise performance of the arrays' blocks including the phase shifters will be important. One can study the noise performance of the presented vector modulator phase shifters and design the phase shifters for an optimum noise performance.

The phase shifters presented in this thesis can be employed in phased arrays operating at K and Ka bands to reduce the arrays' complexity, size, and power consumption.

The limited scan phased array presented in Chapter 4 is amenable for integration, and it can be designed and fabricated using available IC technologies. It should be noted that it is more convenient to design this phased array at mm-wave frequencies where the required constant phase shifts can be provided using compact passive elements. As a prospective application, the presented array architecture can be utilized to design a low-complexity E-band (77 GHz) integrated phased array for applications in long range automotive radars requiring limited scan range. One can also widen the scan range and operation bandwidth of the described phased array using constant delay and negative group delay circuits, respectively, and design an integrated wide-scan phased array operating at 77 GHz for short/long-range automotive radars.

In the K-band integrated phased array presented in Chapter 5, the total number of phase shifters and analog control signals is reduced by a factor of two as compared to conventional phased arrays which use one phase shifter per each radiating element. If the array is intended to operate as a limited-scan phased array, the quadrature generation network and quadrant selector switches can be removed from the circuit, and the power consumption, complexity, size, and cost of the phased array can be further reduced. This K-band phased array can serve as the basis for the design of a low-complexity, integrated, compact, 77 GHz, reconfigurable phased array transceiver for ADAS applications in the future. The 77 GHz phased array can be designed to be reconfigurable for wide-scan and limited-scan operation (for short-range and long-range radar systems) in order to save power.

The presented techniques for designing RF/mm-wave phased arrays with significantly reduced number of phase shifters can be leveraged to simplify electronically-controlled integrated optical phased array architectures. Utilizing phased array architectures with limited number of phase shifters can potentially simplify the architecture and control circuit of optical phased arrays, which will reduce the complexity and cost of optical phased array applications including LIDARs, chemical bio sensing, and imaging.

APPENDICES

APPENDIX A: Analyses of the Phase Shifter Operating Based on the Summation of Rotating Orthogonal Vectors

This section presents the contributions of the phase and amplitude variation of I and Q vectors on the tuning range of the vector sum phase for the phase shifter in Fig. 2.3. The phases of both I and Q vectors given by Eq. I.1 and Eq. I.2 are decreasing functions of C. Therefore, the phase variation range of I and Q vectors corresponding to the variation of C from C_0 to kC_0 is calculated by Eq. I.3.

$$\measuredangle Q = -\tan^{-1}\left(\frac{R(C+C_P)\omega - RCC_PL_P\omega^3}{1 - L_P\omega(C_P\omega + 4C\omega)}\right) \tag{I.1}$$

$$\measuredangle I = -90^\circ - \tan^{-1}\left(\frac{R(C+C_P)\omega - RCC_PL_P\omega^3}{1 - L_P\omega(C_P\omega + 4C\omega)}\right) \tag{I.2}$$

$$\Delta(\measuredangle I) = \Delta(\measuredangle Q) = -\tan^{-1}\left(\frac{R(C_0+C_P)\omega - RC_0C_PL_P\omega^3}{1 - L_P\omega(C_P\omega + 4C_0\omega)}\right) + \tan^{-1}\left(\frac{R(K_cC_0+C_P)\omega - RK_cC_0C_PL_P\omega^3}{1 - L_P\omega(C_P\omega + 4K_cC_0\omega)}\right) \tag{I.3}$$

By satisfying the design conditions in Eq. (2.6) and Eq. (2.9), Eq. (I.3) will be simplified as:

$$\measuredangle Q = -\tan^{-1}\left(\frac{(K_c-1)}{2\sqrt{K_c}}\right) = \tan^{-1}\left(\sqrt{K_c}\right) - \tan^{-1}\left(\frac{1}{\sqrt{K_c}}\right) \tag{I.4}$$

According to Eq. (I.4), for the circuit in Fig. 2.3 which is designed for maximum phase tuning range with a constant output amplitude, half of the total phase tuning range is due to the rotation of I and Q vectors while the other half is owing to the amplitude variation of I and Q.

APPENDIX B: MATLAB Codes for Particle Swarm Optimization Used in the Design of the Four-Element Subarray

The following MATLAB codes utilize particle swarm optimization algorithm to perform task A in Section 4.4.

PSO_4ant.m is the main code that implements PSO algorithm. The user should set the desired range in which the optimal solution will be searched for constant gains of A_is (i=1, 2, 3, and 4) and variable gain amplifiers in lines 8–16 and the maximum phase shift value (φ_{max}) in line 180.

PSO_4ant.m calls the function "PSO_4ant_cost_function.m" which calculates the array factor and, in conjunction with the function pattern_feature.m, characterizes the pattern features including scan angle, side lobe levels, and half power beamwidth error. If the side lobe levels and half power beamwidth meet the criteria defined in lines 4 and 5, the function returns the scan angle.

When optimization is complete, the code displays maximum achievable scan angle and the optimum values for constant gains of A_is and gains of variable gain amplifiers.

PSO_4ant.m

```
clc
clear all
close all
%maximizes cost function, cost function value is scan range in deg.
filename='test.mat'; %for saving results

%Constangt gains range (absolute value)
A1range=[4 8];
A2range=[0 4];
A3range=[0 4];
A4range=[-3 0];
%VGAs gain range (dB)
VGA1range=[-12 -9];
VGA2range=[18 22];
VGA3range=[5 8];
VGA4range=[12 15];

phi=-170; %deg

%PSO parametrs------------------------------------------------------------------
Nrepeat=188; %number of repeats
Nagent=888;  %number of agents
C1=1.49; %particle velocity control
C2=1.49; %particle velocity control
W=linspace(0.6,0.2,Nrepeat);    %W is linearly varied from 0.9 to 0.4 during repeats
dt=1; %displacement/velocity

%PSO variables
SYMIN=[min(A1range), min(A2range), min(A3range), min(A4range), min(VGA1range), min(VGA2range),
min(VGA3range), min(VGA4range)];   %lower bound
SYMAX=[max(A1range), max(A2range), max(A3range), max(A4range), max(VGA1range), max(VGA2range),
max(VGA3range), max(VGA4range)];   %upper bound
dimension=length(SYMIN);     %dimension of solution region

%Generating initial random position and velocity withing the range (position=SY)
position=rand(Nagent,dimension);
velocity=rand(Nagent,dimension);
for m=1:dimension
    position(:,m)=position(:,m).*(SYMAX(m)-SYMIN(m))+SYMIN(m);

    velocity_max=(SYMAX(m)-SYMIN(m))*0.002; %0.1~0.2

    velocity(:,m)=velocity(:,m).*velocity_max;
end

%flag indicating whether the agents are in the solution region or not
%Boundary Flag: 0:in 1:out (boundary condition should be used)
BF=zeros(1,Nagent);
%-------------------------------------------------------------------------------

%optimization begins
waitbar_handle = waitbar(0,'Progress ...');
pbest_fitness=zeros(Nagent,1);
pbest=zeros(size(position));
for repeat=1:Nrepeat
    waitbar(repeat/Nrepeat)
    for agent=1:Nagent
        if(repeat==1)

            %evaluating fitness
            scan_angle_save=PSO_4ant_cost_function(position(agent,:),phi);
            fitness=scan_angle_save;

            %evaluating pbest and global gbest
            pbest_fitness(agent,1)=fitness;
            pbest(agent,:)=position(agent,:);
            if(agent==Nagent)
                [gbest_fitness,index]=max(pbest_fitness);
```

```
            gbest=position(index,:);
            disp(['max scan angle = ', num2str(gbest_fitness), ' deg'])
        end

    else

        if(BF(1,agent)==0)  %checking for invisible boundary
            %current agent is in solution region

            %evaluating fitness
            scan_angle_save=PSO_4ant_cost_function(position(agent,:),phi);
            fitness=scan_angle_save;

            %updating gbest and pbest
            if(fitness>gbest_fitness)
                gbest_fitness=fitness;
                gbest=position(agent,:);
                disp(['max scan angle = ', num2str(gbest_fitness), ' deg'])
            end
            if(fitness>pbest_fitness(agent))
                pbest_fitness(agent)=fitness;
                pbest(agent,:)=position(agent,:);
            end
        else
        end

        %update velocity
        velocity(agent,:)=W(repeat)* velocity(agent,:) + ...
            C1*rand*(pbest(agent,:)-position(agent,:)) + ...
            C2*rand*(gbest-position(agent,:));
        %in each dimension, if abs(velocity) is greater than velocity_max, it
        %must be set to velocity_max.
        for m=1:length(velocity_max)
            if(abs(velocity(agent,m))>abs(velocity_max(m)))
                velocity(agent,m)=sign(velocity(agent,m))*velocity_max(m);
            end
        end

        %update position
        position(agent,:)=position(agent,:)+velocity(agent,:)*dt;

        %checking new position whether is in solution region or not.
        if(sum(position(agent,:)>SYMAX) || sum(position(agent,:)<SYMIN))
            BF(1,agent)=1;
        else
            %this part is necessary for the case when an agnet comes
            %back to the solution region
            BF(1,agent)=0;
        end

    end
  end
end
close(waitbar_handle)

%saving results-----------------------------------------------------------
save(filename)

%Displaying results-------------------------------------------------------
disp(['A1, A2, A3, A4 = ',num2str([gbest(1), gbest(2), gbest(3), gbest(4)])])
disp(['VGA1, VGA2, VGA3, VGA4 = ',num2str([gbest(5), gbest(6), gbest(7), gbest(8)]), 'dB'])
disp(['Max Scan Angle = ',num2str(gbest_fitness),' deg @ Phase Shift = ',num2str(phi),' deg'])

Sin2=1;
b1=Sin2*exp(j*phi*pi/180);
b2=Sin2*exp(j*phi*pi/180);
b3=Sin2*exp(j*phi*pi/180);
b4=Sin2*exp(j*phi*pi/180);
e1=      (1/2)*(10^(0.05*gbest(5)))*(gbest(1)*Sin2+b1);
e2=      (1/2)*(10^(0.05*gbest(6)))*(gbest(2)*e1  +b2);
e3=      (1/2)*(10^(0.05*gbest(7)))*(gbest(3)*e2  +b3);
```

```
e4=(1/sqrt(2))*(10^(0.05*gbest(8)))*(gbest(4)*e3  +b4);

theta=(-90:0.01:90)*pi/180;
AF=e1*exp(j*0*pi*sin(theta))+e2*exp(j*1*pi*sin(theta))+e3*exp(j*2*pi*sin(theta))+e4*exp(j*3*pi*si
n(theta));
AFuniform=exp(-j*0*pi*sin(gbest_fitness*pi/180)).*exp(j*0*pi*sin(theta))+exp(-
j*1*pi*sin(gbest_fitness*pi/180)).*exp(j*1*pi*sin(theta))...
    +exp(-j*2*pi*sin(gbest_fitness*pi/180)).*exp(j*2*pi*sin(theta))+exp(-
j*3*pi*sin(gbest_fitness*pi/180)).*exp(j*3*pi*sin(theta));

figure(5)
plot(theta*180/pi, 20*log10(abs(AF)/max(abs(AF))),'k')
hold on
plot(theta*180/pi, 20*log10(abs(AFuniform)/max(abs(AFuniform))),'--r')
xlim([-90 90])
ylim([-20 0])
xlabel('\theta (deg)')
ylabel('Normalized Array Factor (dB)')
legend('Designed Array','Uniform Array')
```

PSO_4ant_cost_function.m

```
function scan_angle_save=PSO_4ant_cost_function(SY,phi_d)
%phi_d is in deg, scan_angle_save is in deg

SLL_max=-11; %dB
HPBW_error_max=26.28*0.1; %deg (=10% of four-element uniform array's HPBW)
%-------------------------------------------------------------------------
scan_angle_save=0; %rad

A1=SY(1);
A2=SY(2);
A3=SY(3);
A4=SY(4);
VGA1=10^(0.05*SY(5));
VGA2=10^(0.05*SY(6));
VGA3=10^(0.05*SY(7));
VGA4=10^(0.05*SY(8));

phi=phi_d*pi/180;
theta=-pi/2:pi/3600:pi/2;

%Antenna excitations-------------------------------------------------------
Sin2=1;
b1=Sin2*exp(j*phi);
b2=Sin2*exp(j*phi);
b3=Sin2*exp(j*phi);
b4=Sin2*exp(j*phi);
e1=      (1/2)*VGA1*(A1*Sin2+b1);
e2=      (1/2)*VGA2*(A2*e1  +b2);
e3=      (1/2)*VGA3*(A3*e2  +b3);
e4=(1/sqrt(2))*VGA4*(A4*e3  +b4);
%-------------------------------------------------------------------------

AF=e1*exp(j*0*pi*sin(theta))+e2*exp(j*1*pi*sin(theta))+e3*exp(j*2*pi*sin(theta))+e4*exp(j*3*pi*si
n(theta));
[first_null_right,~,first_null_left,~,~,rigth3dB,left3dB]=pattern_feature(AF);
beamwidth3dB=abs(theta(rigth3dB)-theta(left3dB))*180/pi;
AFdB=20*log10(abs(AF)/max(abs(AF)));
SLL=max([AFdB(first_null_right:1:end), AFdB(1:1:first_null_left)]);

[~, index]=max(abs(AF));
scan_angle=theta(index);
AFideal_4antennas=exp(-j*0*pi*sin(scan_angle)).*exp(j*0*pi*sin(theta))+exp(-
j*1*pi*sin(scan_angle)).*exp(j*1*pi*sin(theta))+exp(-
j*2*pi*sin(scan_angle)).*exp(j*2*pi*sin(theta))+exp(-
j*3*pi*sin(scan_angle)).*exp(j*3*pi*sin(theta));
[~,~,~,~,~,rigth3dB,left3dB]=pattern_feature(AFideal_4antennas);
beamwidth3dBuniform=abs(theta(rigth3dB)-theta(left3dB))*180/pi;
```

```
HPBWerror=abs(beamwidth3dB-beamwidth3dBuniform);

if(HPBWerror<=HPBW_error_max & SLL<SLL_max)
    scan_angle_save=scan_angle;
end
scan_angle_save=scan_angle_save*180/pi;

end
```

pattern_feature.m

```
function
[first_null_right,side_lobe_right,first_null_left,side_lobe_left,main_lobe,right3dB,left3dB] =
pattern_feature(AF)
%outputs are indices
absAF=abs(AF); %AF comlex pattern

%main lobe
[~,main_lobe]=max(absAF);

%first null right
for n=(main_lobe+1):1:length(AF)
    if(absAF(n)>absAF(n-1))
        break;
    end
end
first_null_right=n-1;

%first null left
for n=(main_lobe-1):-1:1
    if(absAF(n)>absAF(n+1))
        break;
    end
end
first_null_left=n+1;

%first side lobe right
for n=(first_null_right+1):1:length(AF)
    if(absAF(n)<absAF(n-1))
        break;
    end
end
side_lobe_right=n-1;

%first side lobe left
for n=(first_null_left-1):-1:1
    if(absAF(n)<absAF(n+1))
        break;
    end
end
side_lobe_left=n+1;

%first 3dB right
for n=(main_lobe+1):1:length(AF)
    if((20*log10(absAF(n)))<(20*log10(absAF(main_lobe))-3))
        break;
    end
end
right3dB=n;

%first 3dB right
for n=(main_lobe-1):-1:1
    if((20*log10(absAF(n)))<(20*log10(absAF(main_lobe))-3))
        break;
    end
end
left3dB=n;
end
```

The following MATLAB codes utilize particle swarm optimization algorithm to perform task B in Section 4.4.

PSO_4ant_phi_VGA.m is the main code implementing PSO. The optimum values for constant gains A_is (i=1, 2, 3, and 4), found in task A, should be entered in lines 17–20, and the maximum scan angle and its corresponding phase shift value should also be entered in lines 27 and 28. PSO_4ant_phi_VGA.m calls the cost function "PSO_4ant_cost_function_phi_VGA.m" which calculates the array factor and its features according to the given phase shift and gain values. PSO_4ant_cost_function_phi_VGA.m returns the scan angle if the specified criteria for the side lobe levels and half power beamwidth are satisfied.

When optimization is complete, the gains of the variable gain amplifiers and the phase shift values resulting in different scan angle will be displayed.

PSO_4ant_phi_VGA.m

```
clc
clear all
close all

%PSO initialization-------------------------------------------------------------
%PSO parametrs
Nrepeat=158; %number of repeats
Nagent=585;  %number of agents
C1=1.49; %particle velocity control
C2=1.49; %particle velocity control
W=linspace(0.6,0.2,Nrepeat);    %linearly decrease from 0.9 to 0.4 during repeats
dt=1; %displacement/velocity

filename='test.mat'; %for saving results

%data from optimization for max scan angle
A1=6.4146;
A2=1.3090;
A3=0.1555;
A4=-1.0779;

VGA1=-10.5186;
VGA2=19.6944;
VGA3=6.6919;
VGA4=13.9058;

max_scan_angle=32.5; %deg
phi_at_max_scan_angle=-170; %deg

%-------------------------------------------------------------------------------
scan_angles=max_scan_angle:-0.5:0.5; %deg

phi_desired=(scan_angles/max_scan_angle)*phi_at_max_scan_angle; %linear relation between scan
angle and phi
phi_dev=3; %max deviation from linear profile

VGA1_all=VGA1;
VGA2_all=VGA2;
VGA3_all=VGA3;
VGA4_all=VGA4;
phi_all=phi_at_max_scan_angle;
gain_dev=1; %dB, max deviation from current VGA gain value
max_VGA_gain=30; %max gain for VGAs in dB
min_VGA_gain=-15; %min gain for VGAs in dB

%-------------------------------------------------------------------------------
for sc=2:1:length(scan_angles)
    disp(['current scan angle = ',num2str(scan_angles(sc))])
    iter=1;
    gbest_fitness=10000;

    while(gbest_fitness>0.5 & iter<=3) %checking convergence

        min_VGA1=(VGA1_all(end)-gain_dev)*((VGA1_all(end)-gain_dev)>min_VGA_gain)...
            +min_VGA_gain*((VGA1_all(end)-gain_dev)<min_VGA_gain);
        min_VGA2=(VGA2_all(end)-gain_dev)*((VGA2_all(end)-gain_dev)>min_VGA_gain)...
            +min_VGA_gain*((VGA2_all(end)-gain_dev)<min_VGA_gain);
        min_VGA3=(VGA3_all(end)-gain_dev)*((VGA3_all(end)-gain_dev)>min_VGA_gain)...
            +min_VGA_gain*((VGA3_all(end)-gain_dev)<min_VGA_gain);
        min_VGA4=(VGA4_all(end)-gain_dev)*((VGA4_all(end)-gain_dev)>min_VGA_gain)...
            +min_VGA_gain*((VGA4_all(end)-gain_dev)<min_VGA_gain);

        max_VGA1=(VGA1_all(end)+gain_dev)*((VGA1_all(end)+gain_dev)<max_VGA_gain)...
            +max_VGA_gain*((VGA1_all(end)+gain_dev)>max_VGA_gain);
        max_VGA2=(VGA2_all(end)+gain_dev)*((VGA2_all(end)+gain_dev)<max_VGA_gain)...
            +max_VGA_gain*((VGA2_all(end)+gain_dev)>max_VGA_gain);
        max_VGA3=(VGA3_all(end)+gain_dev)*((VGA3_all(end)+gain_dev)<max_VGA_gain)...
            +max_VGA_gain*((VGA3_all(end)+gain_dev)>max_VGA_gain);
```

```
        max_VGA4=(VGA4_all(end)+gain_dev)*((VGA4_all(end)+gain_dev)<max_VGA_gain)...
            +max_VGA_gain*((VGA4_all(end)+gain_dev)>max_VGA_gain);

        SYMIN=[min_VGA1, min_VGA2, min_VGA3, min_VGA4, phi_desired(sc)-phi_dev];   %lower bound
        SYMAX=[max_VGA1, max_VGA2, max_VGA3, max_VGA4, phi_desired(sc)];   %upper bound
        dimension=length(SYMIN);     %dimension of solution region

        %Generating initial random position and velocity withing the range (position=SY)
        position=rand(Nagent,dimension);
        velocity=rand(Nagent,dimension);
        for m=1:dimension
            position(:,m)=position(:,m).*(SYMAX(m)-SYMIN(m))+SYMIN(m);
            velocity_max=(SYMAX(m)-SYMIN(m))*0.001; %0.1~0.2
            velocity(:,m)=velocity(:,m).*velocity_max;
        end

        %flag for agnets whether are in solution region or not
        %Boundary Flag: 0:in 1:out (boundary condition should be used)
        BF=zeros(1,Nagent);
        %------------------------------------------------------------------------

        %optimization begins
        waitbar_handle = waitbar(0,'Progress ...');
        pbest_fitness=zeros(Nagent,1);
        pbest=zeros(size(position));

        stop_opt=0;
        for repeat=1:Nrepeat
            waitbar(repeat/Nrepeat)
            for agent=1:Nagent
                if(repeat==1)

                    %evaluate fitness
                    % For example: fitness=f(position(agent,:)); where f is cost function
                    scan_angle_save=PSO_4ant_cost_function_phi_VGA([A1, A2, A3, A4,
position(agent,:)]);
                    fitness=abs(scan_angle_save-scan_angle_save(sc));

                    %evaluate pbest for each agnet and global gbest and corresponding fitness
values
                    pbest_fitness(agent,1)=fitness;
                    pbest(agent,:)=position(agent,:);
                    if(agent==Nagent)
                        [gbest_fitness,index]=min(pbest_fitness);
                        gbest=position(index,:);
                        disp(['max scan angle error = ', num2str(gbest_fitness), ' deg'])
                    end

                else

                    if(BF(1,agent)==0)  %checking for invisible boundary
                        %current agent is in solution region

                        %evaluate fitness
                        % For example: fitness=f(position(agent,:)); where f is cost function
                        scan_angle_save=PSO_4ant_cost_function_phi_VGA([A1, A2, A3, A4,
position(agent,:)]);
                        fitness=abs(scan_angle_save-scan_angle_save(sc));

                        %update gbest and pbest
                        if(fitness<gbest_fitness)
                            gbest_fitness=fitness;
                            gbest=position(agent,:);
                            disp(['max scan angle error = ', num2str(gbest_fitness), ' deg'])

                            if(gbest_fitness<1e-10)
                                stop_opt=1;
                                break;
                            end
                        end
                        if(fitness<pbest_fitness(agent))
```

```
                        pbest_fitness(agent)=fitness;
                        pbest(agent,:)=position(agent,:);
                    end
                else
                    if(gbest_fitness<1e-10)
                        stop_opt=1;
                        break;
                    end
                    % % % %             disp('Out of Boundary')
                end

                %update velocity
                velocity(agent,:)=W(repeat)* velocity(agent,:) + ...
                    C1*rand*(pbest(agent,:)-position(agent,:)) + ...
                    C2*rand*(gbest-position(agent,:));
                %in each dimension, if abs(velocity) is greater than velocity_max, it
                %must be set to velocity_max.
                for m=1:length(velocity_max)
                    if(abs(velocity(agent,m))>abs(velocity_max(m)))
                        velocity(agent,m)=sign(velocity(agent,m))*velocity_max(m);
                    end
                end

                %update position
                position(agent,:)=position(agent,:)+velocity(agent,:)*dt;

                %checking new position whether is in solution region or not.
                if(sum(position(agent,:)>SYMAX) || sum(position(agent,:)<SYMIN))
                    BF(1,agent)=1;
                else
                    %this part is necessary for the case when an agnet comes
                    %back to the solution region
                    BF(1,agent)=0;
                end

            end
        end
    end
    close(waitbar_handle)
    iter=iter+1;
end

VGA1_all=[VGA1_all, gbest(1)];
VGA2_all=[VGA2_all, gbest(2)];
VGA3_all=[VGA3_all, gbest(3)];
VGA4_all=[VGA4_all, gbest(4)];
phi_all=[phi_all, gbest(5)];

end
%saving results-----------------------------------------------------------
save(filename)

%Displaying results-------------------------------------------------------
SLL=zeros(size(VGA1_all));
HPBWerror=zeros(size(VGA1_all));
scan_angle=zeros(size(VGA1_all));

theta=-pi/2:pi/3600:pi/2;

for n=1:1:length(VGA1_all)
    phi=phi_all(n)*pi/180;
    VGA1=10^(0.05*VGA1_all(n));
    VGA2=10^(0.05*VGA2_all(n));
    VGA3=10^(0.05*VGA3_all(n));
    VGA4=10^(0.05*VGA4_all(n));

    %Antenna excitations------------------------------------------------------
    Sin2=1;
    b1=Sin2*exp(j*phi);
    b2=Sin2*exp(j*phi);
    b3=Sin2*exp(j*phi);
```

```
    b4=Sin2*exp(j*phi);
    e1=      (1/2)*VGA1*(A1*Sin2+b1);
    e2=      (1/2)*VGA2*(A2*e1  +b2);
    e3=      (1/2)*VGA3*(A3*e2  +b3);
    e4=(1/sqrt(2))*VGA4*(A4*e3  +b4);
    %-------------------------------------------------------------------------


AF=e1*exp(j*0*pi*sin(theta))+e2*exp(j*1*pi*sin(theta))+e3*exp(j*2*pi*sin(theta))+e4*exp(j*3*pi*si
n(theta));
    [first_null_right,~,first_null_left,~,~,rigth3dB,left3dB]=pattern_feature(AF);
    beamwidth3dB=abs(theta(rigth3dB)-theta(left3dB))*180/pi;
    AFdB=20*log10(abs(AF)/max(abs(AF)));
    SLL(n)=max([AFdB(first_null_right:1:end), AFdB(1:1:first_null_left)]);

    [~, index]=max(abs(AF));
    scan_angle(n)=theta(index);
    AFideal_4antennas=exp(-j*0*pi*sin(scan_angle(n))).*exp(j*0*pi*sin(theta))+exp(-
j*1*pi*sin(scan_angle(n))).*exp(j*1*pi*sin(theta))+exp(-
j*2*pi*sin(scan_angle(n))).*exp(j*2*pi*sin(theta))+exp(-
j*3*pi*sin(scan_angle(n))).*exp(j*3*pi*sin(theta));
    [~,~,~,~,~,rigth3dB,left3dB]=pattern_feature(AFideal_4antennas);
    beamwidth3dBuniform=abs(theta(rigth3dB)-theta(left3dB))*180/pi;

    HPBWerror(n)=abs(beamwidth3dB-beamwidth3dBuniform);
end

figure(5)
subplot(2,2,1)
plot(phi_all,scan_angle*180/pi,'k')
xlabel('Phase Shift (deg)')
ylabel('Scan Angle (deg)')
subplot(2,2,2)
plot(phi_all,SLL,'k')
xlabel('Phase Shift (deg)')
ylabel('SLL (dB)')
subplot(2,2,3)
plot(phi_all,HPBWerror,'k')
xlabel('Phase Shift (deg)')
ylabel('HPBW Error (deg)')
subplot(2,2,4)
plot(phi_all,VGA1_all,'k',phi_all,VGA2_all,'b',phi_all,VGA3_all,'r',phi_all,VGA4_all,'g')
legend('VGA1','VGA2','VGA3','VGA4')
xlabel('Phase Shift (deg)')
ylabel('(dB)')
```

PSO_4ant_cost_function_phi_VGA.m

```
function scan_angle_save=PSO_4ant_cost_function_phi_VGA(SY)
%phi_d is in deg, scan_angle_save is in deg

SLL_max=-11; %dB
HPBW_error_max=26.28*0.1; %deg (=10% of four-element uniform array's HPBW)

%-------------------------------------------------------------------------
scan_angle_save=0; %rad

A1=SY(1);
A2=SY(2);
A3=SY(3);
A4=SY(4);
VGA1=10^(0.05*SY(5));
VGA2=10^(0.05*SY(6));
VGA3=10^(0.05*SY(7));
VGA4=10^(0.05*SY(8));
phi=SY(9)*pi/180;

theta=-pi/2:pi/3600:pi/2;
```

```
%Antenna excitations-------------------------------------------------------------
Sin2=1;
b1=Sin2*exp(j*phi);
b2=Sin2*exp(j*phi);
b3=Sin2*exp(j*phi);
b4=Sin2*exp(j*phi);
e1=      (1/2)*VGA1*(A1*Sin2+b1);
e2=      (1/2)*VGA2*(A2*e1  +b2);
e3=      (1/2)*VGA3*(A3*e2  +b3);
e4=(1/sqrt(2))*VGA4*(A4*e3  +b4);
%--------------------------------------------------------------------------------

AF=e1*exp(j*0*pi*sin(theta))+e2*exp(j*1*pi*sin(theta))+e3*exp(j*2*pi*sin(theta))+e4*exp(j*3*pi*si
n(theta));
[first_null_right,~,first_null_left,~,~,rigth3dB,left3dB]=pattern_feature(AF);
beamwidth3dB=abs(theta(rigth3dB)-theta(left3dB))*180/pi;
AFdB=20*log10(abs(AF)/max(abs(AF)));
SLL=max([AFdB(first_null_right:1:end), AFdB(1:1:first_null_left)]);

[~, index]=max(abs(AF));
scan_angle=theta(index);
AFideal_4antennas=exp(-j*0*pi*sin(scan_angle)).*exp(j*0*pi*sin(theta))+exp(-
j*1*pi*sin(scan_angle)).*exp(j*1*pi*sin(theta))+exp(-
j*2*pi*sin(scan_angle)).*exp(j*2*pi*sin(theta))+exp(-
j*3*pi*sin(scan_angle)).*exp(j*3*pi*sin(theta));
[~,~,~,~,~,rigth3dB,left3dB]=pattern_feature(AFideal_4antennas);
beamwidth3dBuniform=abs(theta(rigth3dB)-theta(left3dB))*180/pi;

HPBWerror=abs(beamwidth3dB-beamwidth3dBuniform);

if(HPBWerror<=HPBW_error_max & SLL<SLL_max)
    scan_angle_save=scan_angle*180/pi;
else
    scan_angle_save=10000;
end

end
```

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